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COMSAT TECHNICAL REVIEW

Volume 15 Number 2B, Fall 1985

TDMA: PART I

COMSAT TECHNICAL REVIEW (*NEXT ISSUE*)

Volume 16 Number 1, Spring 1986

TDMA: PART II

Richard R. Colino
Director General,
INTELSAT

Irving Goldstein
Chairman and Chief
Executive Officer,
COMSAT Corporation

Foreword

This special issue of *COMSAT Technical Review* affords us the dual pleasure of saluting the past and greeting the future. The INTELSAT 120-Mbit/s TDMA system is the culmination of over 20 years of work (including research, development, design, field trials, and installations) which led to its current operational status. This project, a real *tour de force* in both engineering and international cooperation, required exceptional skills in the laboratory as well as in the conference room. Because of this, the TDMA INTELSAT project has also been an incubator of leaders, many of whom have gone on to careers of distinction in the communications industries of several countries.

In the forward-looking industry of satellite communications, TDMA constitutes an essential tool for the enhancement of digital satellite communications and for moving further into the new era of worldwide integrated digital services. The expansion of diverse advanced techniques and their introduction and use will enable the INTELSAT system to cope with the competitive future which the communications industry is facing in the 1990s.

As much of the work was done at INTELSAT and COMSAT, it is appropriate for us who have witnessed its development to join hands in presenting this special issue.

Introduction

S. J. CAMPANELLA, G. QUAGLIONE, J. L. DICKS, AND
P. L. BARGELLINI

This special two-part issue of the *COMSAT Technical Review* contains papers on INTELSAT's 120-Mbit/s time-division multiple-access (TDMA) system, which was developed for stations with relatively heavy, typically multidestinational traffic of 100 circuits or more per destination.

The system architecture was developed by a working group of experts from many of the INTELSAT Signatories. From late 1978 to mid-1982, under authorization of the INTELSAT Board of Governors (BG) and its Technical Committee, the working group met many times with Mr. Bruno Drioli of Telespazio as chairman to develop all elements of the system. Close attention to operational details ensured the design of a TDMA system that would provide reliable, fault-free service under conditions of extreme stress.

Design considerations

The working committee studied many design details in depth, including the following:

- choice of bit rate and modulation technique,
- transmission channel design and analysis using the INTELSAT V 72-MHz bandwidth transponders,
- multibeam network acquisition, synchronization, and control,
- traffic burst time plan (BTP) structure and distribution,
- dual reference station architecture for multibeam operation.

- traffic terminal design for multibeam operation,
- network control channel design,
- traffic burst position control by path length delay compensation for traffic terminal location,
- cooperative feedback between traffic terminals and reference stations for burst position control,
- digital speech interpolation (DSI) interfaces accommodating up to eight CEPT-32 primary multiplex interfaces,
- digital noninterpolated (DNI) interfaces accommodating up to 8.192 Mbit/s of digital data transmission in steps of 64 kbit/s,
- Doppler and alignment buffers for terrestrial clock/satellite clock interfaces,
- rate 7/8 Bose-Chaudhuri-Hocquenghem coding for forward error correction (FEC) and detection,
- coordinated BTP change procedure without service interruption, and
- compatibility for satellite-switched (SS)/TDMA operation without traffic terminal modification.

The 4-year effort by the Technical Committee culminated in the preparation and subsequent approval by the BG of the 120-Mbit/s TDMA/DSI System Specification BG-42-65, which has subsequently undergone two revisions.

System development

The point of departure in the development of the specification was the experience gained in the 1978 field trials of a 60-Mbit/s TDMA system in the Atlantic Ocean Region. France, Italy, the Federal Republic of Germany, the United States, and the United Kingdom participated in these tests, which provided valuable information on controlling a network of TDMA terminals, scheduling traffic bursts, synchronizing burst position, measuring bit error rate (BER) performance of burst mode quadrature phase-shift keying (QPSK) in nonlinear transponders, and performing subjective quality assessments of telephone voice transmission with DSI. Tests involving open-loop acquisition and synchronization of traffic burst position led to the control of traffic burst position by transmitting a compensatory propagation delay value to individual stations, which allows precise synchronization at the satellite. Information gathered by these trials provided the basis for the 120-Mbit/s INTELSAT TDMA system design.

On the basis of INTELSAT specification BG-42-65, the introduction of 120-Mbit/s TDMA at the operational level was planned for the Atlantic Ocean Region in the INTELSAT worldwide system. Operational service actually began in the Atlantic Ocean Region in October 1985 between the U.S. and the U.K., followed in December 1985 by service in the Indian Ocean Region on the primary satellite. The TDMA reference terminals in the system, four in each ocean region, were provided by the Nippon Electric Company (NEC) and include a TDMA system monitor built by COMSAT. TDMA traffic terminals are being built by NEC, Mitsubishi, Thomson CSF, M/A-COM Telecommunications, and SPAR, Ltd.

Operation of the 120-Mbit/s TDMA system is supported by the INTELSAT Operations Center TDMA Facility (IOCTF) located in Washington, D.C. The IOCTF, which is connected to all of the TDMA reference stations in the three ocean regions, forms a common network that performs the following tasks:

- disseminates traffic BTPs to all TDMA traffic terminals in all ocean regions,
- commands the execution of coordinated BTP changes, and
- collects and displays critical system status data from the transmission system monitors, and traffic terminal status data from the reference stations.

Future TDMA developments

The 120-Mbit/s TDMA operational system of the INTELSAT V era will be followed by the introduction of the SS/TDMA system in the INTELSAT VI era, which is expected to commence in 1990. Satellite-switched operation has the advantage of providing fully variable interconnectivity among all the beams of a multibeam satellite without the need for transponder hopping, thereby simplifying the operation of traffic terminals. In addition, it allows unconstrained traffic routing in single voice channel increments, leading to significantly improved traffic fill efficiency for the entire system. The greater the number of beams the greater is the potential for savings in terms of improved connectivity and fill efficiency. Introduction of satellite-switched operation in INTELSAT VI will permit operation of the 120-Mbit/s TDMA system with only two reference stations (one primary and one secondary), rather than the four presently required.

At least three new applications of TDMA techniques are being studied for possible introduction during this or the next decade: low-rate TDMA, SS/TDMA networking via an intersatellite link, and video TDMA.

Low-rate TDMA

Implementation of a low-rate TDMA (LR/TDMA) mode with demand assignment can enhance the INTELSAT Business Services Open

Network. Although in the present single-channel-per-carrier/frequency-division multiple-access (SCPC/FDMA) or multiple-channels-per-carrier (MCPC)/FDMA systems, traffic growth can be accommodated by establishing fully connected networks and by allocating variable network capacity among stations, LR/TDMA with its freedom to adjust capacity in the time domain would provide greater flexibility for supporting a variety of user interfaces and data rates.

The main features of the envisaged LR/TDMA system are as follows:

- transmission rate between 3 and 12 Mbit/s,
- coherent QPSK modulation and possibly binary phase-shift keying (BPSK) modulation for small earth stations, and
- FEC coding with a net coding gain of 3 to 5 dB for a code rate of not less than 1/2.

It is expected that such an LR/TDMA system would be controlled at three functionally defined hierarchical levels. Globally, the entire system would be under the supervision of a network control center operated by INTELSAT. Within any given ocean region, at least one synchronization control station per beam would also carry regular traffic. Within a given beam coverage, each traffic terminal would generate its own demand-assignment requests. The network control center would provide the centralized control functions for the dissemination of satellite position information, management of the BTP, processing the demand-assignment requests, and continuous monitoring of network status. Emphasis would be placed on design simplicity, versatility, and the low cost of terminals. Central demand-assignment multiple-access control within a beam coverage could be accomplished by adding this capability to one of the traffic terminals.

Intersatellite link technology

Intersatellite link (ISL) technology could benefit future INTELSAT system configurations by enhancing connectivity. It will be important to investigate the technical features that permit interconnecting multiple SS/TDMA networks via such links. A crucial problem is the synchronization of on-board clocks, which enables a TDMA terminal to treat ISL bursts as if they were local TDMA bursts. The major factors influencing synchronization in an ISL SS/TDMA system are the Doppler shift caused by intersatellite range variation, and the instability of the TDMA terminal clock and of the on-board oscillator which provides switch-state timing.

Two different system design approaches for the synchronization schemes have been suggested. A master-slave correction method uses as reference the clock in the master satellite to synchronize the slave's transmit clock to the on-board switch-state timing through a loopback synchronization window. This ISL transmits reference bursts to the slave satellite. A ground-controlled scheme slaves all on-board clocks to a common, high-stability ground reference clock. Both schemes require an on-board buffer to absorb the timing offsets caused by the distance variation. The minimum buffer size needed is approximately 4 ms, which is equivalent to 480,000 bits of data storage for a 120-Mbit/s burst rate. Thus, memory technologies characterized by high density per chip, low power dissipation, and high resistance to radiation are essential for this kind of application.

Video TDMA

The growth of video traffic in the INTELSAT system has been rapid, much higher than that for telephony. In addition to the conventional demand for occasional-use international television transmission, INTELSAT provides transponder-leased services for television and community antenna distribution, electronic news gathering, video conferencing and telephony, and similar video applications. Since these services in their digital form require a variety of bit rates ranging from less than 1 Mbit/s for teleconferencing video to around 100 Mbit/s for high-definition television, the provision of future video services via an FDMA system which would require different modems for different transmission rates has a number of limitations. The best method of meeting these requirements appears to be a demand-assignment video TDMA system which would provide higher operational flexibility, as well as making available increased capacity to handle system growth.

Previous studies sponsored by INTELSAT indicate the following approaches show considerable promise for possible future video TDMA systems:

a. Two assignment schemes, one for reservation traffic performed by a coordinated BTP change procedure, the other for instantaneous demand traffic based on a single-channel-per-burst method without a coordinated BTP change.

b. Video TDMA terminal equipment designed essentially on the basis of a simplified INTELSAT TDMA terminal, with the addition of a preamble generator signaling channel for demand-assignment control.

c. A simplified synchronization system controlled by only one of the two reference bursts from two reference stations, with each traffic terminal continuously transmitting a synchronization traffic burst regardless of whether or not traffic exists.

d. On-board regeneration with a baseband switch matrix on future satellites to enable small earth stations to participate in the video TDMA transmission system.

Further studies and developments are needed in the areas of earth stations and the universal digital video codec with switchable bit rates and protocols for the demand-assignment procedures, including the case of SS/TDMA operation. To promote penetration of a video TDMA system, it would also be essential to develop low-cost terminals that make extensive and flexible use of large-scale integration circuits.

Advanced satellite concepts

Satellites with many spot beams are another future innovation warranting further study. The need to serve communities of widely distributed, small-aperture, low-power, low-cost earth stations located near the origins of traffic will involve large-aperture satellite antennas used to achieve high values of gain-to-noise temperature ratio and e.i.r.p. To simultaneously achieve the properties of high-gain spot-beam operation and widely dispersed earth stations, the system could consider the use of hopping beams with multiple-frequency TDMA transmission. To accommodate the origins of high-intensity traffic, such a system could use fixed beams with multiple-frequency TDM transmission. One scenario that might be envisaged would consist of two such satellites operating as geostationary orbit gateways, one over the Americas and the other over Europe/Africa, connected by an ISL, to provide a comprehensive, economical international communications network.

Contents of the special issue

In this two-part special issue of the *COMSAT Technical Review*, the first paper explains the architecture of the INTELSAT system. The papers which follow discuss specific aspects of the system and its operation, from terminal acquisition and synchronization, network control facilities, and modem and codec performance, to terrestrial interface architecture and the system monitor. The final paper outlines the advantages of TDMA in the current system and the even greater benefits expected in the INTELSAT VI era through the introduction of SS/TDMA. A note on recent evaluation tests of TDMA/DSI between the United States and the United Kingdom concludes the presentation. A glossary is provided at the end of each part of the issue.

The efforts of all contributors are greatly appreciated and it is hoped that this special TDMA issue will constitute another milestone in the development of satellite communications. Advances in spacecraft design and construction, combined with reduced complexity of the earth segment implementation at large, and in particular progress in solid-state technology in both the digital and analog areas, will make low-cost equipment available for TDMA earth stations on a much broader scale than presently exists.

S. J. Campanella received a B.S.E.E. from the Catholic University of America in 1950, an M.S.E.E. from the University of Maryland in 1956, and a Ph.D. in Electrical Engineering from the Catholic University of America in 1965. He is currently Chief Scientist and Vice President of COMSAT Laboratories. Previously, he served as Executive Director of the Communications Technology Division. He has contributed significantly to technologies for TDMA network control, satellite-switched TDMA, and TDMA terminal development. Dr. Campanella is a Fellow of the IEEE and AAAS. He teaches at George Washington University and holds numerous patents in digital processing techniques.

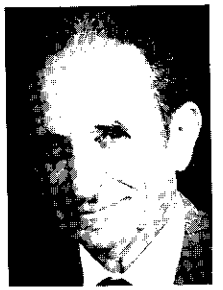
Giuseppe Quaglione graduated from the University of Rome in Electronics Engineering in 1961. After a brief period as Assistant to the Ordinary Professor of Applied Physics at the University of Rome, he joined Telespazio in March 1962, a few months after its foundation. He held responsible positions with Telespazio as Assistant Station Manager of the Fucino earth station, Project Manager of important installations, and Director of Telecommunications Programs, Planning, and International Relations.

Dr. Quaglione is currently Governor for Italy and the Vatican City on the INTELSAT Board of Governors, and has participated since 1966 as the Italian representative to the INTELSAT Advisory Committee on Technical Matters. From April 1973 to June 1977, he was Chairman of this committee (BG/T) with a primary role in INTELSAT V satellite planning, preparation of specifications, and technical evaluation of proposals. He has also been actively involved in preparing the INTELSAT TDMA/DSI specifications, and on several studies related to the introduction of TDMA in the INTELSAT system.

Dr. Quaglione has authored more than 40 technical articles in the field of satellite communications. He is a Senior Member of IEEE and a member of AIAA.

Jack L. Dicks received a B.S. degree in Mathematics and Engineering Physics from Sir George Williams College in Montreal, Canada. He joined the Engineering Division of INTELSAT in 1978 as Manager of the Communications Engineering Department. In this position, he has been responsible for all aspects of the communications systems design and development for both the INTELSAT V and VI satellites and associated earth stations throughout the system. This involved the introduction of many new transmission techniques, both analog and digital, the most notable being development of the 120-Mbit/s TDMA system, which is now being succeeded by SS/TDMA. He has represented INTELSAT on numerous occasions at such ITU forums as the CCIR, and most recently participated in WARC-ORB 85.

Before joining INTELSAT, Mr. Dicks was with COMSAT for 10 years where he was primarily responsible for transmission planning for the INTELSAT III, IV, IV-A, and V satellites. Prior to this, he was on the engineering staff at Teleglobe Canada, responsible for the planning, installation, and testing of submarine cable systems and the introduction of the Mill Village earth station.



Pier L. Bargellini attended the University of Florence and the Polytechnic Institute of Turin, Italy, from which he received the degree of Doctor of Electrical Engineering in 1937. From 1937 to 1948, he worked in Italian communications and electronic industries. In 1948–49, he did graduate work at Cornell University, and from 1950 to 1968 he was with the Moore School of Electrical Engineering, University of Pennsylvania. In 1968, he accepted the position of Senior Scientist in the Director's Office at COMSAT Laboratories, where he remained until his retirement on December 31, 1983.

Dr. Bargellini has authored over 60 publications in U.S. and European technical journals and books. A member of IEEE/IRE since 1937, he was named a Fellow in 1976 and a Life Member of the Institute in 1979. He is an Associate Fellow of the AIAA, a member of the AAS, a Member Emeritus of the AEI, and a member of Sigma Xi and Eta Kappa Nu.

Index: digital transmission; INTELSAT; time division multiple access; modulation, demodulation, modems; speech processing

The INTELSAT TDMA/DSI system

B. A. PONTANO, S. J. CAMPANELLA, AND J. L. DICKS

(Manuscript received September 16, 1985)

Abstract

The INTELSAT 120-Mbit/s time-division multiple-access (TDMA)/digital speech interpolation (DSI) system is described. This system consists of TDMA traffic terminals, TDMA reference and monitor stations, and an INTELSAT Operations Center TDMA Facility (IOCTF). System performance requirements with associated modem characteristics are provided. An overall system description is given illustrating the burst and frame format and explaining the acquisition and synchronization functions. The paper discusses the technical characteristics and interworking of the reference stations and traffic terminals, and describes the traffic terminal interfaces, including DSI. The IOCTF and its coordination functions, such as synchronous burst time plan change, are explained.

Introduction

For more than a decade, INTELSAT has studied the possible use of time-division multiple-access (TDMA)/digital speech interpolation (DSI) in its satellite network [1]–[9]. A series of TDMA/DSI field trials were conducted in 1978 and 1979 which demonstrated that TDMA/DSI circuits operating with DSI gains of 2 and 2.4 gave users a quality of service comparable to that of conventional FDM/FM/FDMA circuits [10]. Most importantly, the field trials demonstrated the feasibility of incorporating TDMA/DSI operation into the INTELSAT network. The results of these tests also indicated a strong need to simplify the equipment design in order to reduce complexity and cost while improving reliability.

TDMA/DSI would first operate with INTELSAT V satellites having spot beams with fixed connectivities, and later with INTELSAT VI and follow-on satellites in a satellite-switched TDMA (SS/TDMA) mode. In either case, the methods of frame acquisition and synchronization would need to operate in a spot-beam environment in which bursts cannot be received by their originating transmitting terminals. Additionally, the transmission system must be compatible with 72-MHz transponders, and must achieve CCIR performance on satellite links which would be interference limited due to a fourfold frequency reuse on INTELSAT V and a sixfold frequency reuse on INTELSAT VI. Finally, the traffic terminals would have to permit eventual use of the 14/11-GHz frequency bands. All of these factors led to a system design which differs significantly from the prototype equipment used for the TDMA field trials [11]–[13].

System overview

The INTELSAT TDMA/DSI system consists of up to eight independent TDMA networks operating in three ocean regions: Atlantic, Indian, and Pacific. Each network comprises four reference stations, a satellite, and a number of traffic terminals. The system will operate with satellites that have four coverage areas: east hemispheric beam, west hemispheric beam, east zone beam, and west zone beam. Zone beam coverage areas will be contained within hemispheric beam coverage areas and use the same frequency band and opposite senses of polarization. Figure 1 shows a satellite with typical east-to-west and west-to-east connectivities of both the zone and hemispheric beams. In this way, two dual-polarized reference stations located in each zone coverage area can monitor and control both zone and hemispheric beam transponders. Each reference station will generate one reference burst per transponder, and each transponder will be served by two reference stations. This arrangement provides redundancy by enabling traffic terminals to operate with either reference burst. The two pairs of reference stations provide network timing and control the operation of traffic terminals and other reference stations.

Some of the reference stations include a TDMA system monitor (TSM) to monitor system performance and diagnose system faults. In addition, the TSM can provide assistance to traffic terminals during lineups.

Traffic terminals transmit and receive bursts containing traffic and system management information. The terminals contain interfaces that connect the TDMA system to the terrestrial networks. The TDMA/DSI system uses two types of interfaces: a DSI interface which accommodates voice traffic and a limited amount of nonvoice traffic, and a digital noninterpolated (DNI) interface which accommodates both data and noninterpolated voice traffic.

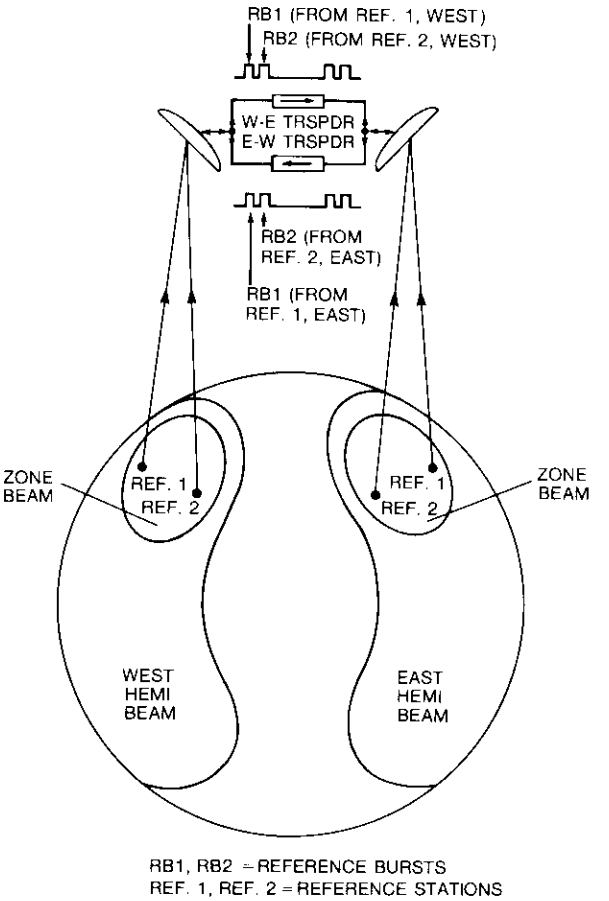


Figure 1. *TDMA System Configuration*

The principal features of the system may be summarized as follows:

a. Frame length is 2 ms.

b. Four-phase, coherent phase-shift keying (CPSK) modulation without differential encoding is employed at a nominal bit rate of 120.832 Mbit/s.

c. Forward error correction (FEC) is applied to the traffic portion of selected traffic bursts.

d. Open-loop acquisition and feedback closed-loop synchronization are used for traffic and reference terminals.

e. Burst time plan (BTP) rearrangement can be performed automatically without loss of traffic.

f. Each pair of reference stations can control up to 60 terminals, including other reference stations.

g. Each traffic terminal can transmit up to 16 bursts and receive up to 32 bursts per frame. One DSI or DNI unit can generate one sub-burst per frame and receive up to eight subbursts per frame.

h. Each traffic terminal can transponder-hop across up to four transponders.

i. A DSI interface can accommodate channel groupings of up to 240 terrestrial channels.

j. A DNI interface can accommodate channel groupings of up to 128 terrestrial channels.

k. Plesiochronous interconnection to the terrestrial network can be provided.

Table 1 summarizes the major functions of the reference stations and traffic terminals.

TABLE 1. REFERENCE STATION AND TRAFFIC TERMINAL FUNCTIONS

REFERENCE STATION FUNCTIONS	TRAFFIC TERMINAL FUNCTIONS
Perform satellite position determination needed for acquisition.	Perform acquisition and synchronization under control of a reference station.
Provide open-loop acquisition information to traffic terminals and other reference stations.	Generate and receive bursts containing traffic and housekeeping information.
Provide synchronization information to traffic terminals and controlled reference stations.	Perform transponder hopping where necessary.
Provide TDMA system monitoring.	Coordinate and implement synchronous burst-time plan changes with the reference station.
Provide network management by transmitting appropriate messages or codes to traffic terminals and other reference stations.	Provide voice and teletype orderwires.
Provide common synchronization across multiple satellite transponders (permitting transponder hopping).	
Provide voice and teletype orderwires.	
Provide access to the IOCTF for network voice and teletype orderwires and for transmittal of status information.	

Transmission system considerations

This section describes the major transmission aspects considered in developing the INTELSAT TDMA/DSI system.

Performance requirements

The INTELSAT TDMA/DSI system is designed to operate with C-band 72-MHz INTELSAT V satellite transponders. Table 2 summarizes the performance requirements which were considered in the transmission design.

TABLE 2. TRANSMISSION DESIGN PERFORMANCE REQUIREMENTS

BER Performance Objective (CCIR Rec. 522)	The bit error rate at the output of the hypothetical reference circuit should not exceed the values of:
	One part in 10^6, 10-min. mean value for more than 20% of any month.
	One part in 10^3, 1-min. mean value for more than 0.3% of any month.
	One part in 10^3, 1-s mean value for more than 0.01% of any year.
Out-of-Band Emission Constraints	$23 - 0.02\ (\alpha - 10)$ dBW/4 kHz at 6 GHz, where α is the elevation angle in degrees.
External Interference Criterion (adjacent satellites and terrestrial)	The aggregate interference power level averaged over any 10 min. should not exceed, for more than 20% of any month, 10% of the total noise power level at the input to the demodulator that would give rise to a BER of one part in 10^6.

The performance objective is specified in order to achieve a clear-sky bit error rate (BER) of 10^{-6}. The amount of up-link fade and down-link carrier-to-noise degradation and the allowable carrier-to-cochannel interference ratios should be such that the BER objective of 10^{-3} is not exceeded for the short-term propagation conditions. The short-term BER objective of 10^{-4} for 0.3 percent of the worst month given in CCIR Recommendation 522 is not considered to be a limiting case.

The out-of-band emission constraints shown in Table 2 relate to the e.i.r.p. of the out-of-band emission that results from spectral spreading of the PSK carrier due to high-power amplifier (HPA) nonlinearities, as well as intermodulation products resulting from multicarrier operation of an HPA. These limits are chosen so as not to degrade the performance of adjacent channels.

The maximum acceptable limit of external interference, given in Table 2, is consistent with the current INTELSAT practice in FDM/FM transmission planning. The total external interference contribution should not exceed 10 percent of the thermal noise level at the demodulator for a BER of one part in 10^6.

An important element in assessing overall link performance for the INTELSAT TDMA/DSI system is the expected modem performance. In a linear system, a Nyquist filter with x/sin x spectrum compensation is considered an optimum modem filter combination. However, this combination may not be optimum when either the earth station HPA or the satellite transponder traveling wave tube amplifier (TWTA) is operated at or near saturation, since the output signal waveform of a nonlinear device is distorted due to AM/AM and AM/PM conversion characteristics. This increases intersymbol interference and generates interfering sidelobes.

Modem design and performance

Based on the results of computer simulations and hardware measurements of various filter combinations, four near-optimum filters (Table 3) were selected for further study. Figure 2 shows the BER performances of the four filter combinations obtained by a computer simulation. The combination of the half-40-percent cosine rolloff with a bandwidth time product, *BT*, of 1 was chosen for both the transmit and receive filters (cases 1 and 2 in Table 3), since this combination provides the best performance in the nonlinear channel and in the modem back-to-back test.

TABLE 3. MODEM FILTER CHARACTERISTICS

	Transmit Filter			Receive Filter		
Case	*BT*	Filter Characteristic	Compensation	*BT*	Filter Characteristic	Compensation
1	1	40% half-cosine	$(x/\sin x)^{1/2}$	1	40% half-cosine	$(x/\sin x)^{1/2}$
2	1	40% half-cosine	x/sin x	1	40% half-cosine	None
3	1.13	30% cosine	$(x/\sin x)^{1/2}$	1	50% cosine	$(x/\sin x)^{1/2}$
4	1.13	30% cosine	x/sin x	1	50% cosine	x/sin x

Various methods of providing compensation were considered with the above filter combinations, and were also examined prior to selection of a particular method. Case 2 of Table 3 shows full compensation of x/sin x applied to the transmit filter, and no compensation at the receiver filter; whereas, case 1 shows half x/sin x compensation applied to both transmit and receive filters. Although the BER performances of cases 1 and 2 are similar, case 2 with full compensation of x/sin x at the transmit side was

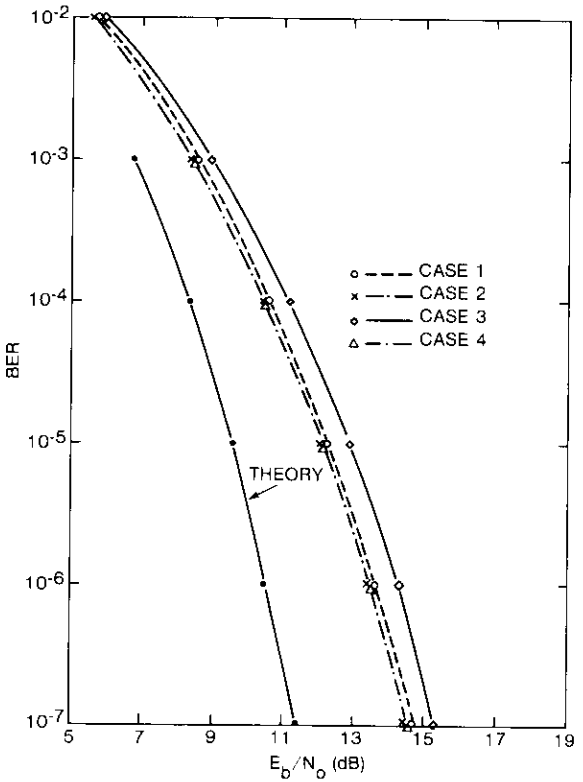


Figure 2. *BER Performance of Filter Combinations*

selected because it simplifies the modem implementation for those using impulse modulators with baseband filtering. For more detail regarding modem design, refer to the paper by Wolejsza *et al.* [14] in this issue.

Spectral spreading

The INTELSAT V TDMA/DSI system is designed to operate with adjacent transponders carrying FDM/FM and TDMA transmissions. When the HPA is operated close to saturation, the regenerated power spectrum causes interference in the adjacent transponders. Since earth stations normally do not provide any filtering at the output of the HPA, the power spectrum spread caused by the HPA spills over into the adjacent transponders.

Figure 3 shows the band spreading due to HPA nonlinearity for the specified modem filter for 4-, 8.5-, and 12-dB input backoffs. The out-of-band emission resulting from the HPA nonlinearity would satisfy the constraints set forth in

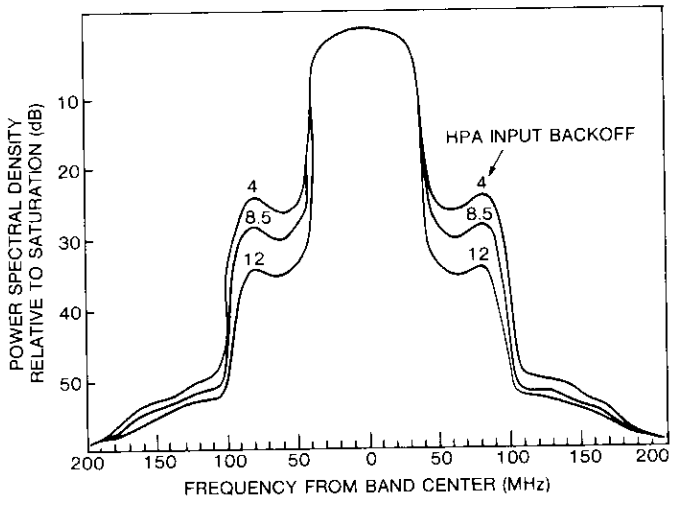


Figure 3. *HPA Output Spectra for the Proposed Transmit Filter*

Table 2 when the HPA is operated with an input backoff greater than 8.5 dB. However, for multicarrier operation, in order to ensure that the intermodulation products do not exceed these constraints, the HPA may also have to be operated with an input backoff greater than 8.5 dB.

Coding requirements

Based on the INTELSAT V TDMA link budgets for clear-sky and rain-degraded propagation conditions, the performance required for the FEC code is derived from Figure 4. A number of coding schemes were examined in terms of performance, hardware complexity, and their suitability for INTELSAT V TDMA application. Figure 5 gives the performance of several of these schemes. Based on cost, risk, and performance considerations, the rate 7/8 BCH code was selected. This code is a (128, 112) double error correcting and triple error detecting code.

System description

This section provides a functional description of the TDMA burst and frame structure, the method of acquiring and synchronizing TDMA bursts, and the TDMA system requirements and associated benefits of transponder hopping.

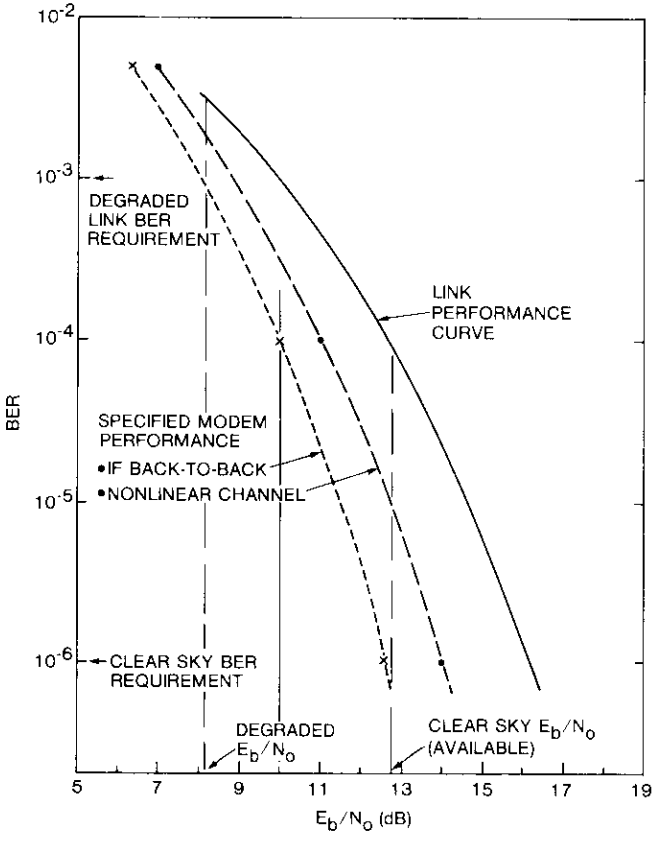


Figure 4. *Derivation of the FEC Coding Performance Requirements*

Burst and frame format

Figure 6 shows the structure of the TDMA frame, which contains reference bursts and traffic bursts. RB1 and RB2 designate the two reference bursts in the frame. Each reference burst is generated by a separate reference station and under normal conditions both reference stations are active. One station is designated the primary reference station, the other the secondary (back-up) reference station. The TDMA terminals receive the secondary reference station only when the primary reference station fails. The minimum guard time between bursts is 64 symbols, which ensures that bursts will not interfere with each other because of inaccuracies in the synchronization system.

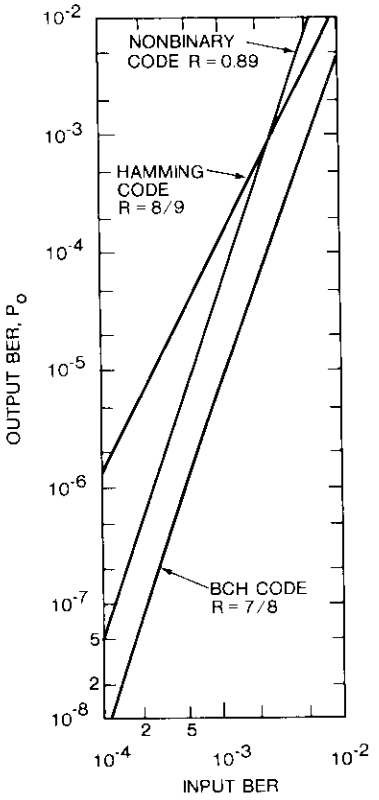
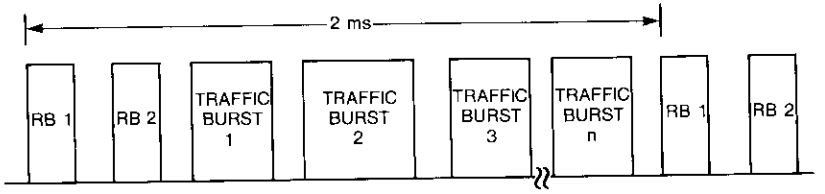


Figure 5. *Performance Curves of FEC Codes*



RB 1: REFERENCE BURST FROM REFERENCE STATION 1.
RB 2: REFERENCE BURST FROM REFERENCE STATION 2.

Figure 6. *Structure of TDMA Frame*

Figure 7 shows the structure of the burst format for both the reference and traffic bursts. The reference burst comprises a preamble and a control and delay channel (CDC). The preamble consists of five parts: the carrier and bit timing recovery sequence, the unique word, the teletype orderwire channels, the service channel, and the voice orderwire channels. The traffic burst consists of the preamble and a traffic section made up of DSI and/or DNI sub-bursts.

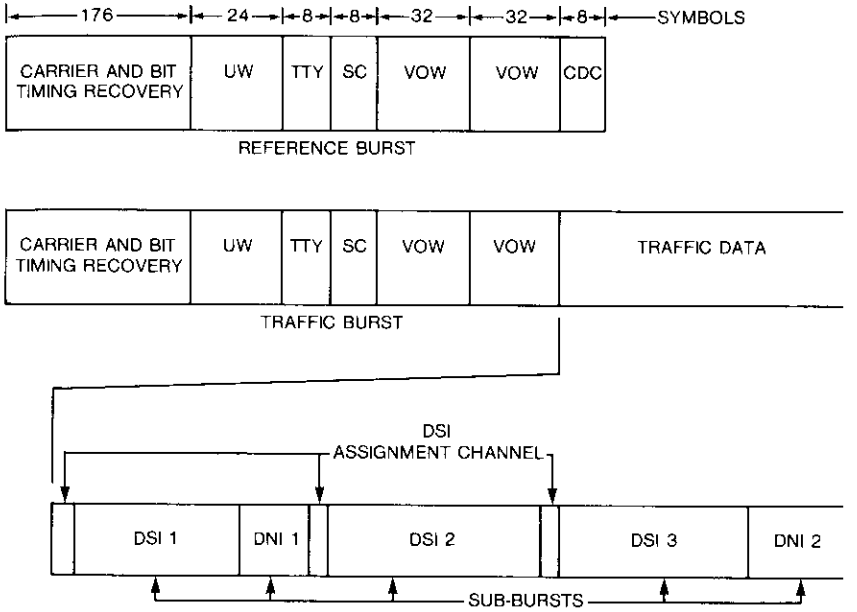


Figure 7. *Burst Format*

The carrier and bit timing recovery sequence is designed to enable the modem to acquire and synchronize to received bursts. The 24-symbol unique words are used to differentiate between reference bursts and traffic bursts, resolve the fourfold phase ambiguity inherent in QPSK modulation, and mark the beginning of a multiframe. Eight teletype orderwires and two voice orderwires are allocated 8 symbols and 64 symbols, respectively, in each reference burst and traffic burst. Eight symbols form a service channel which is used to exchange control and housekeeping information throughout the TDMA network. Finally, in the reference burst, eight symbols are allocated for the CDC, which is used to control the traffic terminal's acquisition and synchronization.

The 24-symbol unique word contains two consecutive 12-symbol patterns which serve three purposes. The last symbol of a word marks the position of a burst relative to the start of the frame. Next, the pattern of the first 12 symbols is used to resolve the fourfold phase ambiguity. Finally, the pattern of the second 12 symbols relative to the first is an identifier used to distinguish between reference bursts and traffic bursts. For 15 consecutive frames, all bursts use the same identifier (UW0), but on the 16th burst (called a multiframe marker) the identifier changes to identify the burst as RB1, RB2, or a traffic burst. A multiframe is defined as the 16 frames starting with the multiframe marker. Figure 8 shows the multiframe format.

The unique word missed detection probability for the INTELSAT TDMA system is specified to be less than 1×10^{-8} at $E_b/N_o = 7$ dB in an IF back-to-back loop with a unique word detection threshold of 5. In a nonlinear channel, the unique word missed detection probability is specified to be less than 1×10^{-8} at $E_b/N_o = 8$ dB.

The eight symbols allocated to the service channel carry the types of messages shown in Table 4. A service channel message consists of an 8-bit function code, a 22-bit parameter, and a 2-bit parity check, which together form a 32-bit codeword. This word is transmitted over one multiframe (16 TDMA frames) at a rate of 2 bits per frame. For protection against errors, each bit is repeated eight times in every burst.

The CDC in the reference burst is used to control TDMA traffic terminals for acquisition and synchronization. The CDC cyclically addresses each control traffic terminal and reference station in successive multiframes using a 32-multiframe cycle referred to as a control frame. A 32-bit CDC message (Figure 9) is transmitted in a manner similar to that of the service channel message. Except for terminal number 0, which is used for reference station status codes and the BTP number, each message is destination-directed to the particular terminal identified by the terminal number. These destination-directed messages control terminal operation by means of a 2-bit control code and a 22-bit word that provides the transmit delay.

Acquisition and synchronization

Acquisition is the process by which a TDMA terminal initially places its burst into the assigned position within the TDMA frame. This process must be executed without interference to other bursts in the frame. A terminal may enter the acquisition phase if it receives, via the CDC, an acquisition control code from the reference station, together with a value of transmit delay. The transmit delay is the time between the reception of a reference burst and the transmission of the acquiring terminal's own burst. The reference

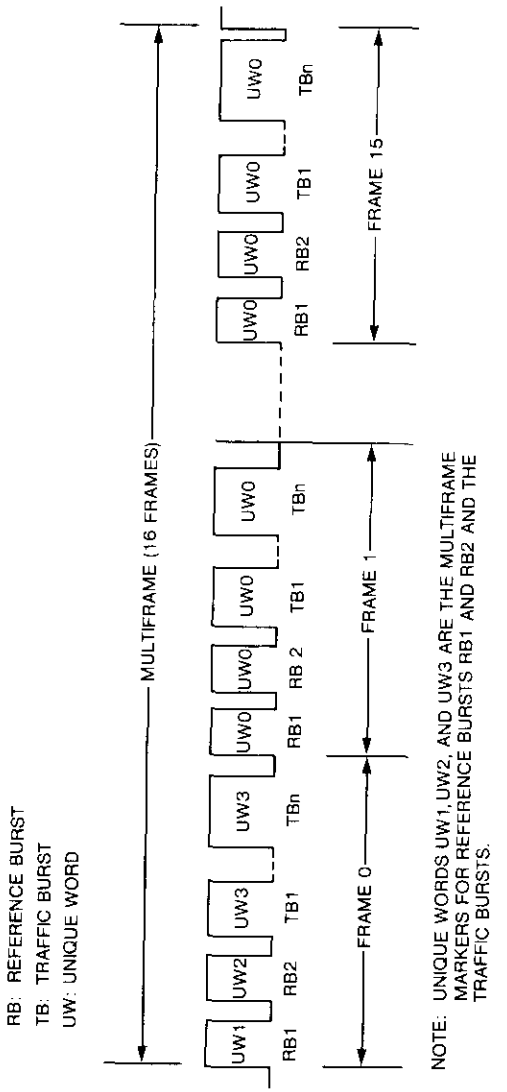


Figure 8. *Multiframe Format*

TABLE 4. SERVICE CHANNEL MESSAGES

FUNCTION CODE (8 bits)	TYPE	CONTENTS OF THE PARAMETER DATA BLOCK (22 bits)		TRANSMISSION PRIORITY[a]
		FIRST 8 BITS	LAST 14 BITS	
00000000	Ineffective Message	Not Used	Not Used	Fifth
00000001	Transmission of Delay Used (from all terminals)	Value of Delay Used	Value of Delay Used	First
	Burst Time Plan			
00000010	Request for "Ready to Change" (from primary reference station to selected terminals)	Terminal Number	New BTP Number	NA[b]
00000011	"Ready to Change" (from selected terminals)	Terminal Number	New BTP Number	Third
00000100	Notification of BTP change (from primary reference station to all terminals)	Countdown 00010000 00001111 — 00000001 00000000	Not Used	NA[b]
	Alarms			
00000101	High-BER Alarm (from traffic terminals to traffic terminals)	Terminal Number	Burst Number	Fourth
00000110	Unique Word Loss Alarm (from traffic terminals to traffic terminals)	Terminal Number	Burst Number	Second
00000111	Selective Do Not Transmit Code (SDNTX) (from reference station to selected traffic terminal)	Terminal Number	Burst Number[c]	NA[b]

[a]For traffic terminals.
[b]Not applicable for traffic terminal transmission.
[c]Code 111111111111 for the burst number is used to switch off all bursts transmitted by the terminal.

station calculates the value of the transmit delay based on a knowledge of satellite position. This method is referred to as "open-loop" acquisition.

Either of two methods of satellite position determination can be employed. One method uses TT&C data to generate a set of coefficients which can be used to predict the satellite position for periods of up to several days. These

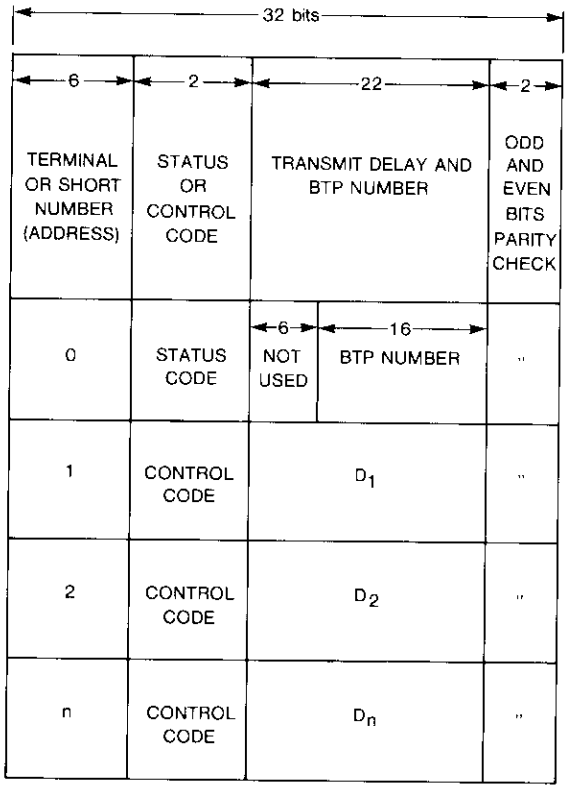


Figure 9. *CDC Structure*

coefficients are updated and sent to the reference stations, which use them to calculate satellite position. This method is capable of predicting satellite position to within 1 km. The other method of satellite position determination uses ranging data taken from either the reference stations or the cooperating traffic stations. These data, values of transmit delay (D_n), are a by-product of the synchronization process.

During the acquisition process, the terminal transmits only its preamble (short burst). The reference station measures the position of the short burst within the frame and transmits a new value of delay which causes the short burst to move to its nominal position. When the reference station has verified that the short burst is in its nominal assigned position, the station transmits the synchronization code to the terminal. Reception of the synchronization code notifies the terminal that the acquisition phase is complete and that traffic sub-bursts can be added to the preamble.

Synchronization is the process by which bursts are maintained in their assigned position within the frame. The reference station monitors the position of the burst in the frame and continuously modifies the transmit delay values to maintain the bursts in their proper positions. This process is referred to as "feedback closed-loop" synchronization. A more detailed description of acquisition and synchronization is given by Forcina and Bedford [15] in this issue.

Transponder hopping

Transponder hopping permits improved traffic interconnectivity with minimal hardware complexity in a nonglobal beam system such as the INTELSAT V. The traffic terminals are designed to hop across a maximum of four transponders, which can be separated in frequency and/or polarization. Since the TDMA/DSI system employs mutually synchronized reference bursts in all transponders, traffic bursts transmitted into different transponders will be separated by fixed time intervals. This allows reference stations to control the position of only one of the terminal's bursts, since the others are synchronized by fixed time offsets.

TDMA reference and monitor stations

Each TDMA reference and monitor station (TRMS) consists of reference terminal equipment (RTE) and in some cases a TSM. The TRMS equipment was developed and built by Nippon Electric Corporation (NEC), with the TSM being manufactured by COMSAT as a subcontractor to NEC. The RTE provides network timing and controls the operation of traffic terminals and the other reference stations. The reference stations also provide timing and control for synchronized BTP changes. The TSM is used to monitor system performance, diagnose system failures, and assist users in executing their traffic terminal lineups.

Each reference station is equipped with sufficient redundancy to provide a high degree of reliability. However, in order to satisfy INTELSAT's continuity of service criteria, each reference station operating in a given coverage area will have one backup reference station. This leads to the concept of two reference bursts per frame (primary and secondary). Although one of the two stations has a standby role, both stations are simultaneously active. In the event of a failure in the primary reference station, system control passes to the secondary reference station without disturbance to the network.

Figure 10 is a general block diagram of the RTE. The RTE equipment consists of two on-line signal processing equipment (SPE) units, a local timing source, a control and display console (CADC), and an engineering service circuit (ESC) subsystem. An SPE will accommodate up to four transmit and receive chains. Transponder hopping at the IF or RF level is not employed at reference stations, and consequently, each up- and down-chain is equipped with separate modems. Each signal processing unit generates reference bursts,

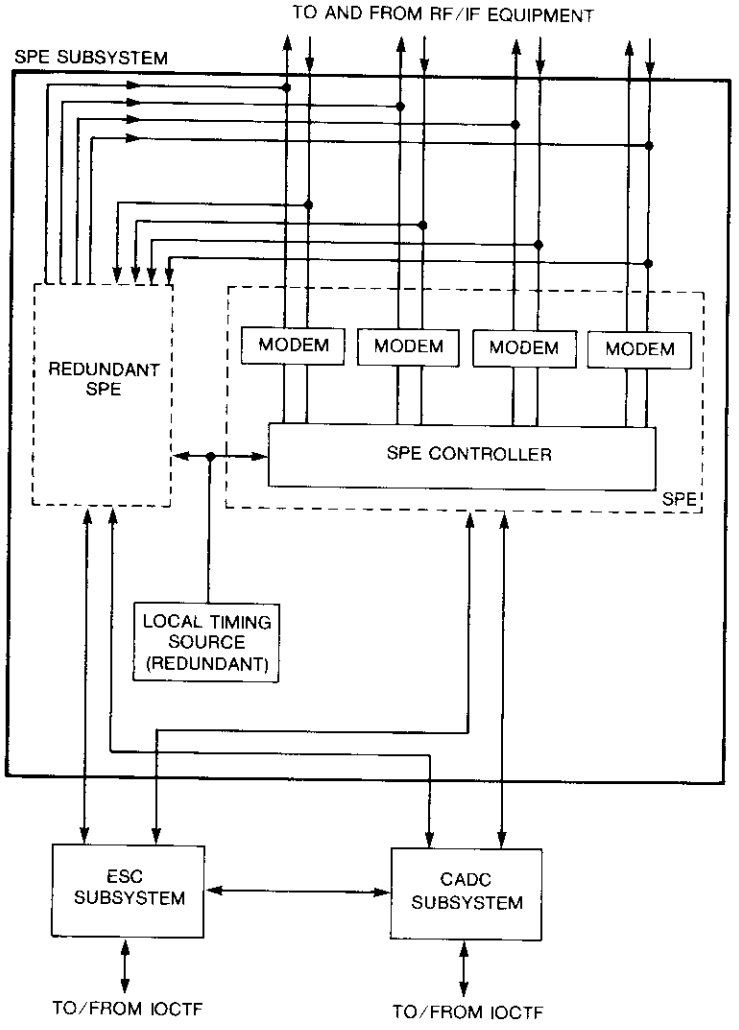


Figure 10. *RTE Configuration*

but the output of only one of the units is selected for transmission. The other unit serves as an active backup.

To detect abnormalities in its own operation, each SPE is equipped with a monitor and diagnostics (MAD) unit which monitors a number of SPE conditions. Upon detection of a failure condition, the standby SPE is switched on-line. The switchover to redundant RF/IF equipment is controlled by local switchover logic which is independent of the MAD unit. Since the switchover time of the local redundancy is considerably shorter than that of the RTE switchover unit, no interaction occurs between the RF/IF equipment and the RTE.

The CADC provides the operator interface to the RTE equipment. Local equipment status and TDMA system status are provided on video display units (VDUs) in the display console. The local equipment status displays include mimic diagrams of equipment configuration, protocol status, and a facility for examining the events which led to a failure condition. This display continuously stores the last 4 s of the state of the protocols within the terminal. The system status displays include lists of controlled stations and their current status, events during a BTP change, and the status of all four reference stations in the network, together with a facility for examining the event which led to a traffic station failure.

The ESC subsystem provides voice and data communications over the TDMA network for all reference and traffic stations. This facility is extended by leased voice-grade circuits to the INTELSAT Operations Center TDMA Facility (IOCTF), and not only provides day-to-day communications, but also serves as the principal means for the IOCTF to disseminate the TDMA BTPs to the reference and traffic stations.

The TSM is designed to measure relative burst power level, burst carrier frequency, burst position, pseudo BER, and transponder input backoff. The system monitor data can be displayed locally, and is also accessible for display at the IOCTF. Operation of the monitor can be controlled locally or remotely from the IOCTF.

Figure 11 is a block diagram of the TSM. The measurement subsystem is sequenced through the various reference station down-chains by the VHF switch. For each down-chain, burst measurements are gated by the TDMA controller. The measurement data are processed within the TSM processor prior to display, storage, and transmission to the IOCTF. The performance requirements of the TSM are presented in Table 5. A more complete description of the implementation and its operation will be given by Barnett *et al.* [16].

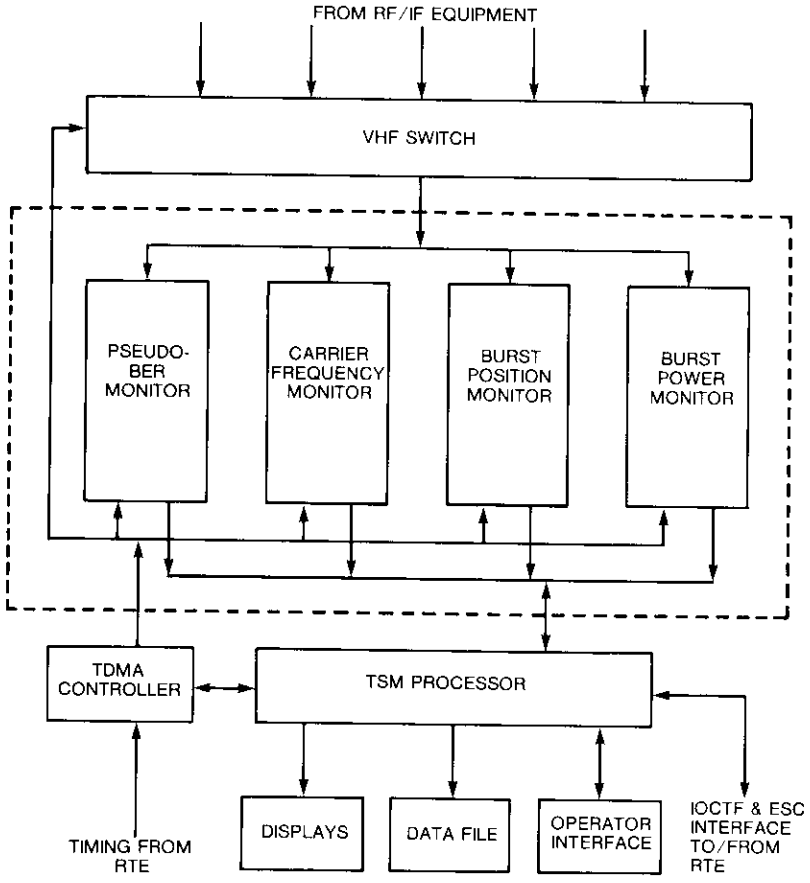


Figure 11. *TDMA System Monitor*

TABLE 5. TSM PERFORMANCE REQUIREMENTS

PARAMETER	ACCURACY
Relative Burst Power Level	±0.25 dB
Carrier Frequency	
Reference Burst	±3 kHz
Traffic Burst	±0.2 kHz
Burst Position Error	±1 symbol
Pseudo BER (over 10^{-2} to 10^{-6} range)	±20%
Transponder Operating Point	±1 dB

Traffic terminals

Traffic terminals are used by INTELSAT's signatories to route their voice and data traffic through the INTELSAT TDMA system. The traffic terminals are procured by signatories from a variety of manufacturers, who build the equipment to INTELSAT performance specifications.

The traffic terminals are required to acquire and synchronize to the frame under the control of a reference station. Once synchronized, the terminal transmits bursts and sub-bursts in accordance with a BTP prepared by INTELSAT. The sub-bursts, which contain the traffic from that station, originate from either DSI or DNI units.

Digital speech interpolation unit

Most traffic uses DSI to make the most efficient use of satellite capacity. DSI takes advantage of the intermittent nature of speech by assigning satellite channels only to active voice channels. Each DSI interface unit can accommodate up to 240 terrestrial channels. The usable capacity of the DSI unit may vary from one terrestrial channel to its maximum capacity in increments of one terrestrial channel. The corresponding maximum capacity of a DSI unit is 127 satellite channels, with the actual utilization varying from one satellite channel to its maximum capacity. Individual DSI units may be designed for either multidestination or single-destination operation. Units operating in the multidestination mode are capable of transmitting to eight destinations in one sub-burst and receiving eight sub-bursts.

Each DSI sub-burst contains an assignment channel (DSI-AC) located at the beginning of the sub-burst and occupying 128 bits (equivalent to one satellite channel). The assignment channel carries assignment messages and DSI alarm messages. Assignment messages are used to inform the receive-side DSI unit of the terrestrial-channel-to-satellite-channel associations made at the transmitting side. The DSI-AC consists of 128 bits which carry three 16-bit assignment messages. Rate 1/2 Golay coding is used to correct all 1-, 2-, and 3-bit errors. This coding is used on all links, unlike rate 7/8 BCH channel coding which is only used on selected worst-case links. Figure 12 depicts the structure of the DSI-AC.

Each DSI unit contains a special assignment channel check procedure which is used to check automatically the end-to-end DSI channel assignments. The procedure consists of a special channel on the transmit side of the DSI which generates a request for assignment once every 10 s. At the receive side, a special receive channel expects to receive the assignment every 10 s. If assignment is not received, an alarm is raised and sent back to the originating DSI unit.

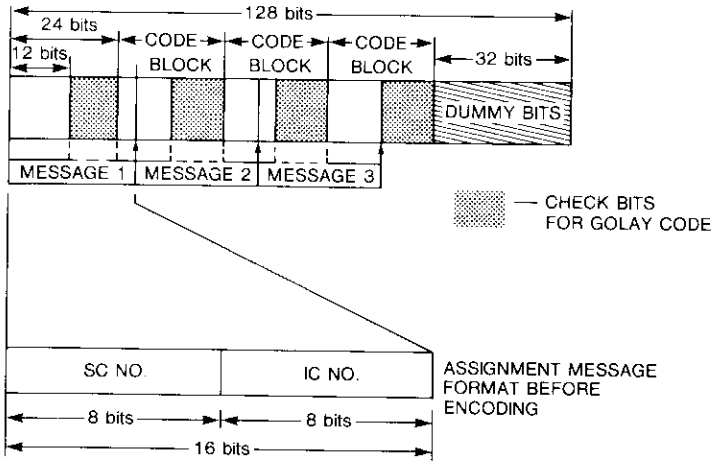


Figure 12. *Structure of DSI Assignment Channel*

The ratio of the number of terrestrial channels to the number of satellite channels to be employed by each DSI unit in the system will be set such that competitive clipping lasting more than 50 ms will occur on less than 2 percent of the voice spurts. To meet this requirement while maximizing satellite capacity, the DSI units employ bit reduction. When the number of simultaneously active terrestrial channels exceeds the number of satellite channels allocated for the DSI units, additional satellite channels can be derived by "stealing" the least significant bit of the 8-bit voice channels. These overload channels are used to prevent *freeze-out*, where no satellite channel is available for an active terrestrial channel. This process reduces the affected satellite channels from 8 bits to 7 bits during periods of overload.

The DSI unit may be used to carry noninterpolated traffic by preassigning terrestrial channels to satellite channels. The noninterpolated channels are transmitted at the end of the sub-bursts and the number of channels is expandable in one-channel steps to a maximum of 127 satellite channels. A detailed description of the INTELSAT DSI system is given by Rieser and Onufry [17] in this issue.

Digital noninterpolated units

Small-capacity links and preassigned data can be accommodated by a DNI unit. The capacity of a DNI unit may range from 1 to 128 satellite channels in single-channel increments. The DNI unit may also be used for forming higher bit rate channels in increments of 64 kbit/s up to a maximum of 8.192 Mbit/s.

Terrestrial interfaces

The INTELSAT system uses the plesiochronous method for interconnecting national digital networks. The networks are interconnected by means of buffers sized to accommodate the surplus or deficiency of bits arising from the difference in bit rates between two networks. This is accomplished by repeating a block of pulse-code modulation (PCM) bits if the buffer is nearing depletion, or deleting a block if the buffer is full. The block length is chosen to be equal to the PCM frame period, since deleting or repeating PCM frames (termed slipping) will not cause significant disturbance to the network.

To further limit the disturbance, slipping is only allowed every 72 days (CCITT Rec. G.811). This in turn dictates that the national networks and the TDMA frame rate must be held to within one part in 10^{11} of their design frequencies over 72 days. Therefore, one reference station must derive its frame timing from a high-stability clock which provides the time reference for the TDMA network.

Plesiochronous interfacing of the TDMA terminals also requires the use of Doppler buffers to remove path length variations caused by satellite movement. The TDMA/DSI system buffers can accommodate up to 1.1 ms of peak-to-peak path length variation.

INTELSAT Operations Center TDMA Facility and system coordination

As an organizational focal point for the TDMA system, the IOCTF controls, coordinates, and helps maintain the correct operation and interworking of each TDMA network within the system. To support these activities, the IOCTF performs the following major functions:

a. monitoring of RTEs, and hence TDMA networks, through the use of high-speed data lines, and
b. voice and teletype (TTY) communications to each RTE and traffic terminal in each network.

Figure 13 shows the overall TDMA system configuration. The IOCTF can operate with up to eight TDMA satellite networks and is coupled to each reference station in the network via voice-grade packet-switched data links. A network packet recirculator/concentrator (NPRC) is provided for each network. The output of NPRC forms an interface between each satellite network and the IOCTF. In addition, each reference station serves as a gateway terminal for the TDMA voice and TTY ESC system, and is connected to the IOCTF via leased voice circuits.

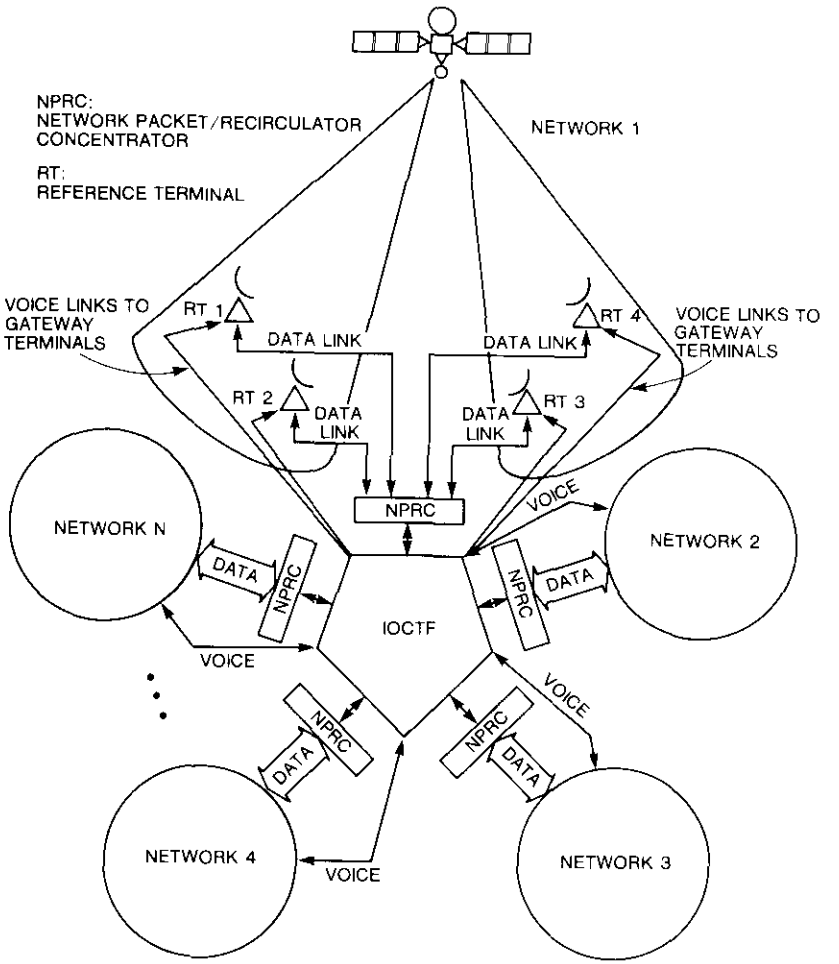


Figure 13. *Overall TDMA System*

Operators at the IOCTF monitor and to some degree control the status of the RTEs and the associated TDMA networks. The monitoring capability is derived from the transfer of displays and alphanumeric data from the RTEs to the IOCTF via the data lines. IOCTF operators can thus view the operation of the network from the perspective of any or all RTEs. This unique perspective allows the operators to assist in providing maintenance support for RTEs and traffic terminals. This perspective also allows a limited amount of remote

control, specifically the coordination of synchronous time plan changes and system startup following an outage. In both cases, commands and responses are exchanged over the data lines. In addition, the IOCTF utilizes the ESC voice orderwire (VOW) TTY circuit to verbally control all significant terminal activities that can affect TDMA system operation. Finally, the IOCTF generates, stores, distributes, and verifies critical BTP information which configures the operation of each reference and traffic terminal in the network. For details on the design of the IOCTF, refer to the upcoming paper by Hodge *et al.* [18].

System coordination

System coordination functions are concerned with facilitating and maintaining the correct operation and interworking of the TDMA network. These functions are in three groups: VOW TTY communications, interterminal alarms, and automatic burst time rearrangements.

Orderwires

The TDMA system provides for two independent voice orderwires and up to eight independent TTY orderwires on each transmitted traffic and reference burst. These circuits are used by the terminal operators to coordinate commissioning, operation, and fault finding of the equipment. Automatic signaling and call routing are provided by switching computers in each earth station. The IOCTF gains access to each network by using the reference stations' switching computers as gateway exchanges. This gives the IOCTF full voice and TTY communications with all reference and traffic terminals in the TDMA system.

Alarms

All TDMA terminals are capable of exchanging two types of alarms corresponding to loss of unique word and the occurrence of a high BER on a received burst. The alarms are selectively addressed to the terminal originating the burst, using the service channel. Unique word alarms are generated when a particular burst's unique word is declared lost for more than 500 ms. The alarm message is sent every second until the unique word is declared present. High-BER alarms are generated whenever a burst is perceived to have an error rate worse than 1×10^{-3}. This alarm message is sent every 4 s until the BER improves.

The reference stations have the capability within the display equipment to log all alarm conditions, and can assist traffic terminal operators in diagnosing faults. The reference station displays are made available to the IOCTF, which can also log the alarm incident and assist in fault finding, especially when a larger scale network problem exists.

BTP distribution and change

A BTP for the INTELSAT system contains all the operational parameters for all the terminals in the network. Each BTP is represented by a unique number, and current time plan number verification is part of a terminal's acquisition procedure. Thus, whenever a BTP change occurs, all stations must be updated.

To ensure that critical elements of the BTP have been correctly loaded into the terminals, critical elements are grouped into a special format and transmitted over a secure data circuit using the CCITT X.25 data protocol, which provides error correction and automatic repeat request (ARQ) facilities. When successfully received, the data are translated into a form suitable for use by the terminal and stored in the background memory which will be used to control the terminal. These data will then be retransmitted back to the IOCTF to enable the operators to perform a bit-by-bit comparison with the original transmission.

The INTELSAT TDMA/DSI system provides fully synchronous, real-time BTP arrangements. This involves changing the position and/or length of some or all bursts within the frame of any TDMA transponder. Immediately prior to the implementation of a new BTP, the controlling primary reference station sends a "start of plan change" message to the primary in the other coverage area. After an appropriate delay which synchronizes the messages, both reference stations send a "request for ready to change" message to the terminals over the service channel (Figure 14). This message activates a facility which permits the terminal to react to a countdown signal. When this facility is activated, the terminal transmits a "ready to change" signal over the service channel. When both reference stations have confirmed that all terminals involved in the time plan change are enabled and the new time plan has been correctly placed in the background memories of the terminals concerned, the other reference stations declare "ready to change." To inform the controlling reference station that it is ready to change, the other reference station sends a message over the service channel for 1 s. When the controlling primary station receives this message, it declares "ready to initiate countdown."

Figure 15 shows the BTP rearrangements sequence. The controlling reference station sends "initiate countdown" to the reference station, and after delays necessary to synchronize the countdown, both stations send "notification of time plan change" to all terminals using a countdown sequence over the service channel. When terminals receive the final countdown message, they

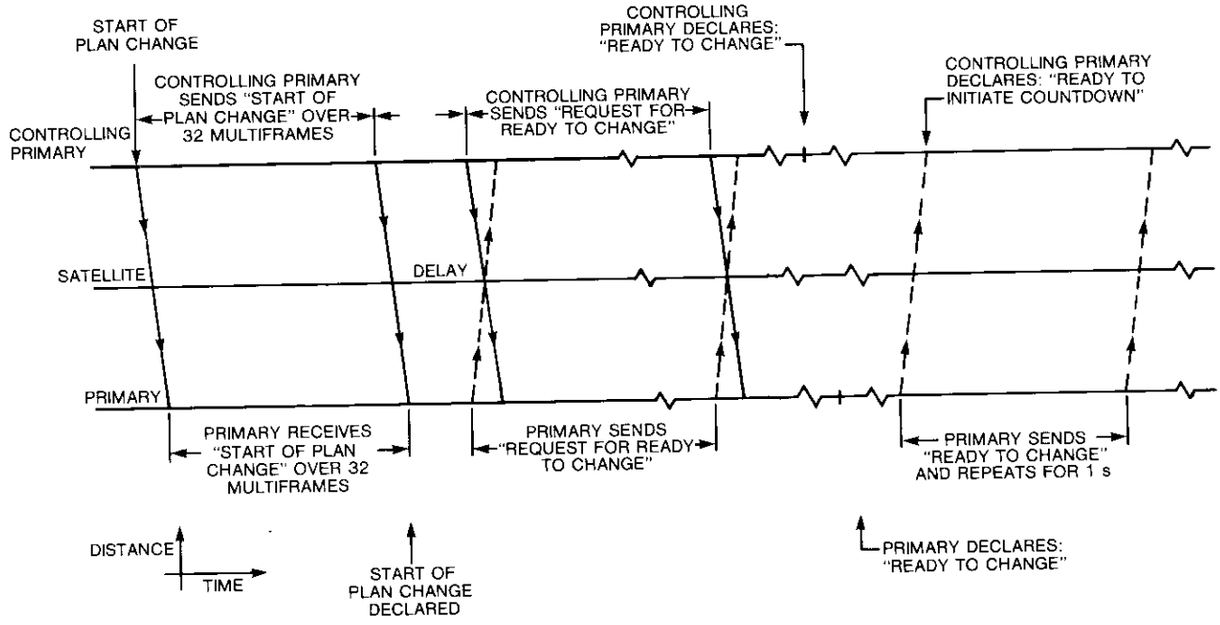


Figure 14. *Preparation for BTP Change*

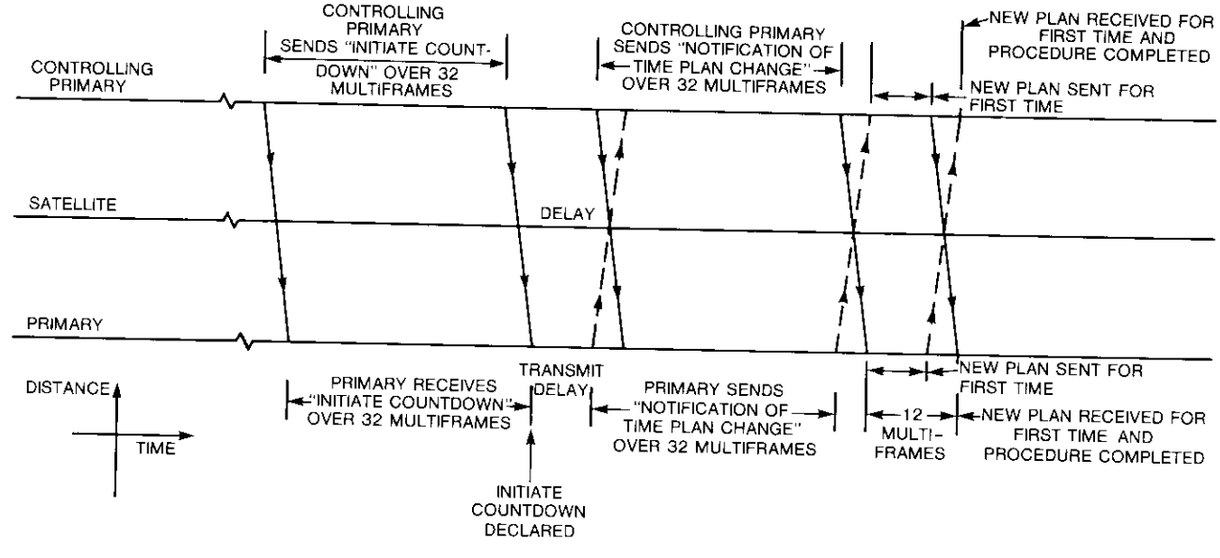


Figure 15. *BTP Change Timing Diagram*

adopt the new transmit time plan on the next transmitted frame, while on the receive side, the plan is adopted 12 multiframes after the final message. This results in a synchronized system-wide change without interruption to the network.

Conclusions

With the introduction of the 120-Mbit/s TDMA system, INTELSAT has reached a major milestone in system evolution. The incorporation of TDMA/DSI into the system increases voice channel efficiencies by a factor of approximately 3 over conventional FDMA with frequency modulation. The TDMA system currently operates on the INTELSAT V satellites having hemispheric and zone antenna beams with fixed connectivities, and the system design allows for eventual operation with the INTELSAT VI satellites in a dynamic SS/TDMA mode.

With terrestrial networks converting to digital operation on a worldwide basis, the INTELSAT TDMA/DSI system offers a common link which can effectively provide direct interconnections between networks of this type. By the early 1990s it is foreseen that a major portion of INTELSAT traffic will be carried by TDMA/DSI. The use of either 32- or 16-kbit/s low-rate voice encoding will likely be introduced to further enhance the system with an additional increase in channel efficiency.

Acknowledgments

The INTELSAT TDMA system was developed by many individuals from all parts of the world. Contributors included INTELSAT staff members, INTELSAT signatories, COMSAT Laboratories personnel, and equipment manufacturers, all of whom worked hard to make INTELSAT TDMA a reality.

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[18] G. D. Hodge *et al.*, "TDMA Network Control Facility," scheduled for publication in *COMSAT Technical Review*, Vol. 16, No. 1, Spring 1986.

Benjamin A. Pontano received a B.S.E.E. degree from Carnegie-Mellon University in 1965, and M.S.E.E. and Ph.D. degrees from the Pennsylvania State University in 1967 and 1970, respectively. He originally joined COMSAT Laboratories in 1969, and was appointed Manager of the Laboratory Simulation Branch. He rejoined COMSAT Laboratories in 1984, and is currently a Principal Scientist engaged in the study of future satellite systems for domestic and international applications. During the interim, Dr. Pontano was with INTELSAT for over 10 years, where he was actively involved in development of the INTELSAT TDMA system and design of the INTELSAT VI spacecraft system.

S. J. Campanella received a B.S.E.E. from the Catholic University of America in 1950, an M.S.E.E. from the University of Maryland in 1956, and a Ph.D. in Electrical Engineering from the Catholic University of America in 1965. He is currently Chief Scientist and Vice President of COMSAT Laboratories. Previously, he served as Executive Director of the Communications Technology Division. He has contributed significantly to technologies for TDMA network control, satellite-switched TDMA, and TDMA terminal development. Dr. Campanella is a Fellow of the IEEE and AAAS. He teaches at George Washington University and holds numerous patents in digital processing techniques.

Jack L. Dicks received a B.S. degree in Mathematics and Engineering Physics from Sir George Williams College in Montreal, Canada. He joined the Engineering Division of INTELSAT in 1978 as Manager of the Communications Engineering Department. In this position, he has been responsible for all aspects of the communications systems design and development for both the INTELSAT V and VI satellites and associated earth stations throughout the system. This involved the introduction of many new transmission techniques, both analog and digital, the most notable being development of the 120-Mbit/s TDMA system, which is now being succeeded by SS/TDMA. He has represented INTELSAT on numerous occasions at such ITU forums as the CCIR, and most recently participated in WARC-ORB 85.

Before joining INTELSAT, Mr. Dicks was with COMSAT for 10 years where he was primarily responsible for transmission planning for the INTELSAT III, IV, IV-A, and V satellites. Prior to this, he was on the engineering staff at Teleglobe Canada, responsible for the planning, installation, and testing of submarine cable systems and the introduction of the Mill Village earth station.

Index: communication satellites, digital transmission, synchronization, INTELSAT, time division multiple access

An experimental TDMA traffic terminal*

R. P. RIDINGS, R. R. LINDSTROM, AND T. R. DOBYNS

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Abstract

Basic concepts, critical design issues, and implementation criteria for an experimental 120-Mbit/s time-division multiple-access (TDMA) traffic terminal developed by COMSAT Laboratories per INTELSAT Specification BG-42-65 (Rev. 2) are presented. The terminal consists of a TDMA controller, modem, digital speech interpolation (DSI) module, and special test equipment. The architectures of the TDMA controller, operator console, DSI interface, and the special test equipment are illustrated. The special test equipment consists of a reference burst generator and a bit error rate/error-free interval measurement unit. The reference burst generator makes it possible to perform tests in a satellite loop configuration. Speed of operation, especially in regard to the unique word detector and the forward error correction unit, was a critical item in the terminal design. Other critical items were the interfacing of 32 DSI modules to the TDMA controller, and the design of a receive-side retiming unit with a demodulator interface which required no clocks after the last symbol of data. The impact of the COMSAT Laboratories terminal and its support in the INTELSAT 120-Mbit/s TDMA system implementation are also dealt with.

Introduction

The 120-Mbit/s time-division multiple-access (TDMA) traffic terminal developed by COMSAT Laboratories to verify the INTELSAT operational

*This paper is based on work performed at COMSAT Laboratories under the joint sponsorship of the Communications Satellite Corporation and the International Telecommunications Satellite Organization (INTELSAT). Views expressed are not necessarily those of INTELSAT.

protocols of Specification BG-42-65 (Rev. 2) [1] incorporates a new design approach for the 120-Mbit/s forward error correction (FEC) codec. A bus approach for interconnecting the TDMA terminal with a large number of digital speech interpolation/digital noninterpolation (DSI/DNI) modules was developed. In the DSI module, particular development effort was focused on an adaptive threshold speech detector. Special attention also was given to the unique word (UW) detector and its operational reliability at the 60.416-MHz* data rate. Testing and verification were performed in conjunction with the development of a reference station emulator (RSE) [2]. Several of the designs developed for the laboratory terminal have been incorporated into the operational TDMA equipment of the U.S. Signatory.

Summary of the INTELSAT TDMA system

The BG-42-65 (Rev. 2) traffic terminal uses INTELSAT V satellites operating at 6/4 GHz with 72-MHz bandwidth hemi- and zone-beam transponders. The system specifications are summarized in Table 1. Redundancy in the event of a reference terminal failure is provided by primary and secondary reference terminals in a designated transponder. Traffic terminals transmit and receive bursts from two types of terrestrial interfaces: DSI interfaces, used primarily for voice traffic, and DNI interfaces used primarily for data traffic. Traffic terminals normally take timing and control from the primary reference terminal; however, if a terminal fails to receive the primary reference burst for a given period of time, it will switch and take timing and control from the secondary reference terminal.

TABLE 1. TDMA SYSTEM FEATURES

Bit Rate	120.832 Mbit/s
Frame	2 ms
Multiframe	32 ms (16 frames)
Control Frame	1.024 s (32 multiframes)
Modulation	Four-phase PSK
Demodulation	Coherent
Phase Resolution	Unique word
Acquisition	Open loop
Synchronization	Control from reference terminal
Unique Word Length	24 symbols
BTP Change	Synchronized
FEC	128/112 BCH code

*Hereafter referred to in the text as 60 MHz.

Reference terminals send control information to traffic terminals in the control and delay channel (CDC), addressing control information to a specific terminal in a designated multiframe once a control frame (1 s). Each reference burst addresses the same terminal in the same multiframe. Both reference and traffic terminals communicate network supervision information in the service channel (SC). The CDC and SC messages are sent at 2 bits per 2-ms frame over a 16-frame multiframe (32 ms).

Traffic terminal description

This description covers the architecture of the TDMA controller, operator console, DSI interface, and special test equipment consisting of a reference burst generator and a bit error rate/error-free interval (BER/EFI) measurement unit. The burst modem and the DSI/DNI module are discussed in other papers in this issue [3], [4].

Figure 1 is block diagram of the traffic terminal equipment. The baseband traffic is digitally encoded into 8-bit, A-law companded pulse-code modulation (PCM) at the channel banks and sent to the DSI module in CEPT 2.048-Mbit/s serial format. The DSI module interfaces a maximum of 240 input channels to an allocated number of satellite channels based on the speech activity in the presence of speech the channel. An adaptive speech detector determines

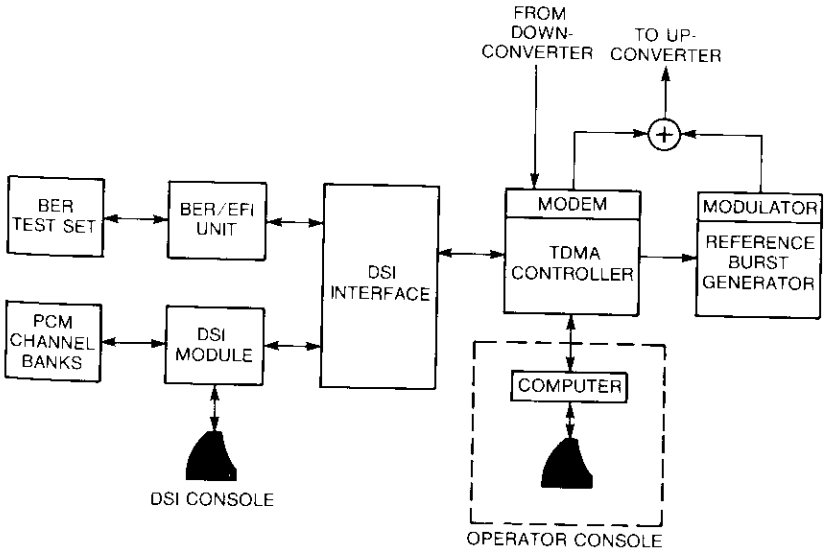


Figure 1. *Traffic Terminal Block Diagram*

in the channel, and if speech is detected the input channel is connected to an available satellite channel. The DSI traffic is then stored in compression memories located in the DSI interface. The controller reads the compression memories, thereby multiplexing the traffic into TDMA bursts which are transmitted at 120.832 Mbit/s using four-phase phase-shift keying (PSK) modulation. The receive traffic is demultiplexed from the TDMA burst and routed through the DSI interface to the expansion memory located in the DSI module. The digitized traffic is then converted back to analog at the PCM channel banks.

The TDMA terminal is monitored and controlled from an operator console consisting of a CRT, keyboard, and minicomputer. Special attention was given to the monitor displays to ensure that all real-time information accurately reported terminal status, an especially important feature when the terminal is used to evaluate network protocol performance. In order to trace fault conditions, the minicomputer stores time-tagged test results with terminal status conditions. In addition, the minicomputer stores a number of burst time plans (BTPs) for various test scenarios.

A reference burst generator was included to provide a stand-alone test system independent of the INTELSAT reference stations. It transmits primary and secondary reference bursts with the necessary protocols for acquiring and synchronizing traffic bursts in IF, RF, and satellite loop configurations. It also has the capability of testing the acquisition and synchronization protocols of the TDMA controller.

End-to-end link performance was analyzed in terms of the BER and EFIs. The BER/EFI measurement unit used during field testing of the terminal [5] interfaces a continuous-mode BER test set to the TDMA controller, enabling BER and EFI measurements on the traffic portion of the TDMA burst. The EFI data were stored on a floppy disk for later analysis.

TDMA controller

Performance of the TDMA controller is measured in terms of its ability to achieve and maintain synchronization, accept new BTPs, and interface traffic data to the DSI modules. This unit controls transmit start time, preamble generation, FEC coding, and data scrambling, in addition to supplying control signals to the RF equipment for transponder hopping. It generates apertures* for detecting UWs, descrambles received data, and processes orderwire channels.

Figure 2 is a functional block diagram of the TDMA controller. Digital data are received from the demodulator in two serial bit streams, P and Q, at a

*An aperture is a 65-symbol interval within which UW detections are allowed.

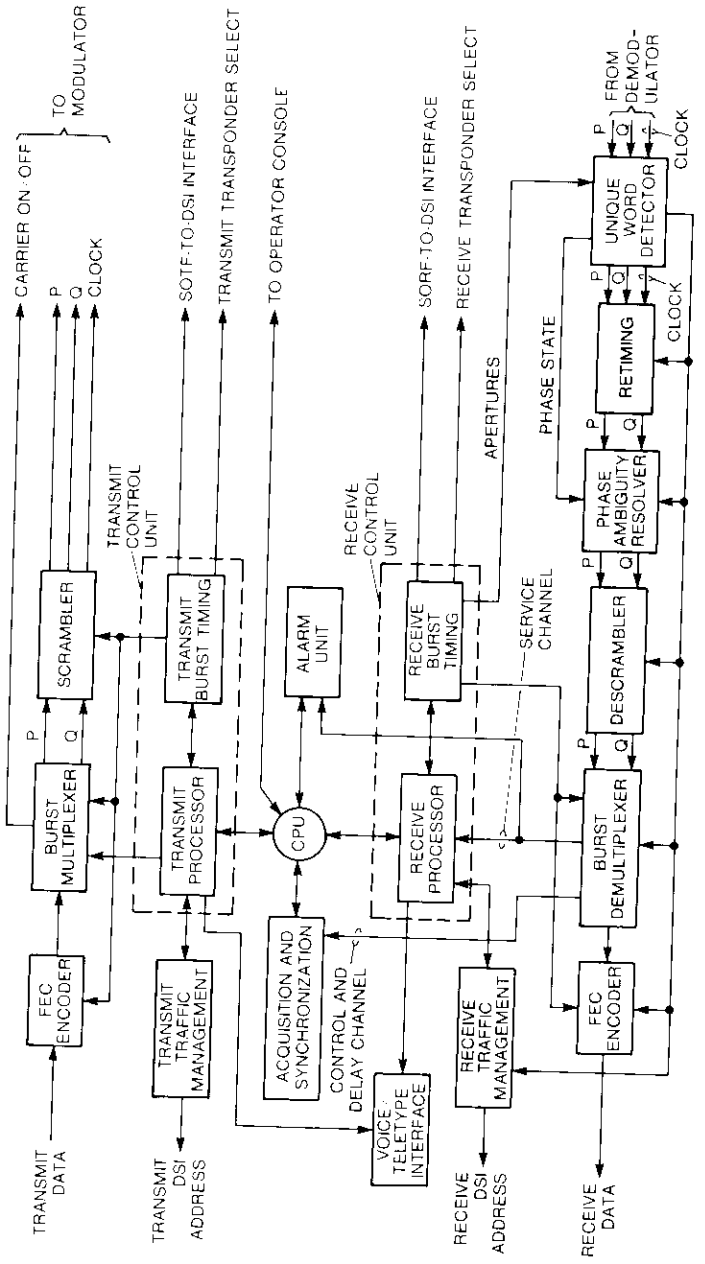


Figure 2. *TDMA Controller Functional Block Diagram*

60-MHz rate. The P and Q data and the receive 60-MHz clock are fed to the UW detector and phase ambiguity resolver. Once the UW has been detected, the phase can be resolved. The retiming circuit reclocks the P and Q data from the recovered modem 60-MHz clock to the local 60-MHz clock. The UW detect signal resets the retiming circuit prior to retiming the received data. The recovered clock is generated in the demodulator during the received burst, and the retiming circuit eliminates the need for residual clock cycles trailing the received burst.

The output of the retiming circuit consists of the P and Q data, synchronous with the continuous local 60-MHz clock, which are descrambled and sent to the demultiplexer and FEC decoder. UW detection synchronizes the timing for the descrambling process, the demultiplexing, and FEC decoding. The received burst is demultiplexed (8-bit parallel) into the following components: voice orderwire (VOW), teletype orderwire (TTYOW), SC, CDC (from reference station only), and traffic data. The receive traffic management unit routes the traffic data to the correct terrestrial interface module (TIM) in the DSI interface unit. The VOW and TTYOW are sent to their respective units. The reference burst SC and CDC are sent to the acquisition and synchronization (A&S) unit, while all traffic burst SCs are sent to the receive control unit and alarm unit.

The transmit TDMA burst is assembled in the burst multiplexer under command of the burst timing signals. The carrier and bit timing recovery (CBTR) sequence and the UWs are read from read-only memory (ROM). The UW is followed by the SC, voice and teletype orderwires, and traffic data. The burst multiplexer multiplexes the data in an 8-bit parallel format before conversion to two 60-Mbit/s serial bit streams labeled P and Q.

The traffic management unit multiplexes the data from the DSI TIMs into the TDMA bursts. This unit assigns the data to the particular burst and to the sub-burst within the burst. The entire traffic data portion of the burst is FEC-encoded upon selection, and after the UW all data are scrambled. The P and Q data, the continuous 60-MHz clock, and the carrier on/off signal are sent to the modulator.

The control unit consists of a central processing unit (CPU) and A&S unit, plus transmit and receive timing units. The BTP information is entered at the operator console, converted into a hardware-compatible format, and sent to the transmit and receive control units via the CPU. The BTP information is then loaded into foreground and background memories which interface to the transmit and receive burst timing and traffic management hardware. The foreground/background memory configuration enables the terminal to implement a BTP change without disrupting the transmit or receive traffic. Due to satellite Doppler and the difference between the local station and reference station 60-MHz clocks, the transmit and receive timing must be corrected to

maintain synchronous operation of the TDMA network. The A&S unit, together with the CPU, implements both the reference burst identification and A&S routines given in Section 6 of BG-42-65 (Rev. 2). Receive frame timing is controlled by the time of reception (UW detection) of the controlling reference burst. Transmit frame timing is controlled by receiving delay, D_n, information from the reference station in the CDC. Transmit frame synchronization is maintained by implementing the received D_n value every control frame.

MICROPROCESSOR NETWORK

The real-time processing tasks required in the TDMA controller were assigned to a distributed network of six Z-80 microprocessors in order to meet the processing speed requirements, simplify software development, and facilitate the connection between hardware and software. The Z-80 microprocessor network is shown in Figure 3, and the tasks assigned to each processor are listed in Table 2.

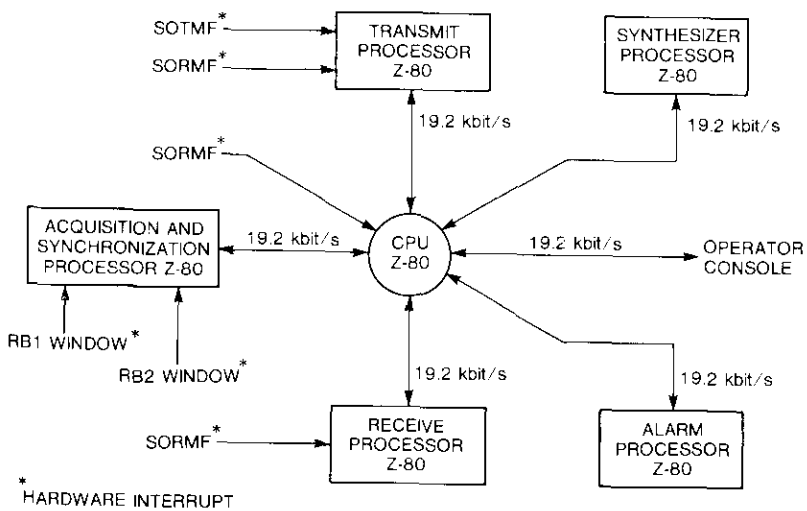


Figure 3. *Z-80 Microprocessor Network*

The CPU controls the transfer of information between processors and communicates with the operator console. A 19.2-kbit/s asynchronous serial interrupt-driven communications interface is used between processors. This serial link is implemented using RS-422 between the operator console and the CPU, and RS-232 between the processors. A parity bit on the data blocks

TABLE 2. MICROPROCESSOR FUNCTIONS

A&S	Implements the network control protocol for TDMA terminal acquisition and synchronization.
CPU	Controls receive front panel displays. Controls interprocessor communications. Communicates with operator console. Controls transmit front panel displays. Monitors terminal. Changes BTP countdown.
TRANSMIT	Loads transmit BTP into timing memory and traffic management memory. Implements D_n. Controls BTP change for transmit hardware. Implements SDNTX and DNTX messages. Processes transmit SC messages.
RECEIVE	Loads receive BTP into timing memory and traffic management memory. Controls BTP change for receive hardware. Computes high BER and UW loss for received traffic bursts.
ALARM	Processes SDNTX messages. Processes high BER and UW loss messages.
SYNTHESIZER	Performs control functions for generating independent 2.048-MHz transmit and receive clocks (locked to SOTF and SORF, respectively) for the DSI units.

provides error detection capability. The interrupt priority establishes the foreground communications for sending CDC and SC information from the A&S and alarm processors, respectively, to the CPU and the transmit processor. All other communications are considered background and are temporarily halted to ensure the transfer of the CDC and SC information. The speed of interprocessor communications could be increased by replacing the serial communications links with a high-speed parallel multiprocessor bus.

The real-time tasks implemented by the microprocessors are synchronized with the hardware by using the interrupt signals shown in Figure 3. The A&S processor is interrupted by the reference burst 1 (RB1) and reference burst 2 (RB2) window signals generated each frame period in the receive timing unit. These interrupts signal the A&S processor to read the CDC and SC data from the received reference bursts. Additional information is read informing the processor of a reference burst UW detection, UW violation, and multiframe identification. The transmit processor is interrupted by the start-of-receive multiframe (SORMF) generated in the receive timing unit and the start-of-transmit multiframe (SOTMF) generated in the transmit timing unit. The receive processor is interrupted by the SORMF. These interrupts provide multiframe timing for interprocessor communications, implementing the received D_n, reading SC data, and counting multiframes for a BTP change as described in Section 8 of BG-42-65 (Rev. 2).

ALARM FUNCTIONS

The alarm functions indicate failures in the TDMA controller which can initiate an automatic switchover to a redundant unit. Fault detection and redundancy switching are important aspects of the TDMA controller design because an undetected failure can cause an outage of all TDMA traffic. The COMSAT Laboratories TDMA traffic terminal, which is an experimental prototype, does not incorporate redundancy, although the following alarm functions are implemented:

- hardware failures,
- software failures (watchdog timers),
- loss of receive frame synchronization (RFS),
- loss of transmit frame synchronization (TFS),
- transmit frame acquisition (TFA) error,
- "do-not-transmit" (DNTX) message received in reference burst CDC,
- high BER and UW loss alarm messages received in traffic burst SC,
- high BER and UW loss measurements on received traffic bursts, and
- "selective-do-not-transmit" (SDNTX) message received in reference burst SC.

The high BER and UW loss alarm messages received in the traffic burst SC are processed in accordance with Subsection 7.5 of BG-42-65 (Rev. 2). The UW loss and high BER measurements are implemented in the receive processor. The BER is measured on the UW, and when a UW miss occurs (more than five bit errors), it is assumed that six errors have occurred. When a UW loss alarm occurs, the high BER measurement is deactivated. With each BER and UW loss measurement alarm, the appropriate message is sent to the originating traffic station via the transmitted SC.

When an SDNTX alarm message is received, the designated burst(s) will cease transmission, and operator intervention is required in order to reestablish transmission (BG-42-65, Rev. 2, Subsection 7.6). If the SDNTX messsage is all 1's, the terminal will cease transmission of all bursts in the given transponder. If the principal burst is designated by the SDNTX message, the terminal will cease transmission of all bursts.

The traffic terminal alarm status will be displayed in real time on the operator console. To prevent the invalid occurrence of alarms prior to terminal synchronization, all SDNTX messages, high BER alarms, and UW loss alarms will not be processed until transmit frame synchronization is established.

DSI interface

The DSI interface unit provides the connectivity between the DSI modules and the TDMA controller. It houses a TIM for each DSI module and the frequency synthesizers for the DSI clocks. The transmit portion of the TIM contains a compression memory which stores a sub-burst of DSI data in an 8-bit parallel format at a 2.048-Mbit/s rate. The transmit traffic management unit reads 8-bit samples from the compression memory at a 15.104-MHz rate and multiplexes each sub-burst of data into the TDMA burst. The received sub-bursts are directed to the proper DSI by the receive traffic management unit. The TIM then forwards the received sub-burst directly to the DSI module in an 8-bit parallel format at a 15.104-MHz rate.

The frequency synthesizers generate the transmit and receive 2.048-MHz clocks. The clocks are locked to the transmit frame timing and receive frame timing, respectively. A phase-locked loop, controlled by the synthesizer processor, is used to lock a voltage-controlled crystal oscillator to the frame timing.

Operator console

The purpose of the operator console is to allow efficient management of the traffic terminal by the operator. The functions summarized in Table 3 were developed after careful study of the 120-Mbit/s TDMA network operation, previous experience in field testing COMSAT Laboratories' 60-Mbit/s TDMA system [6], and field testing of the 120-Mbit/s TDMA terminal at the Andover, Maine, earth station [5]. The operator console is implemented using a DEC PDP 11-04 minicomputer, a DEC VT-100 video terminal, and a DEC dual high-density floppy disk unit.

TABLE 3. OPERATOR CONSOLE FUNCTIONS

MONITORING	Real-time display indicating traffic terminal status and alarms.
CONTROL	Provides commands at keyboard for complete terminal control.
BTP GENERATION	Keyboard entry of BTP.
DATA LOGGING	Logging of terminal status and alarms. Time tagging all events.

The TDMA controller is monitored from the real-time status display shown in Figure 4, consisting of receive acquisition and steady-state reception, RFS, and transmit frame A&S information, including D_m. These protocols are explained in Section 6 of BG-42-65 (Rev. 2).

TIME 11:03:33	STATUS DISPLAY		DATE 01-03-85		
ALARM STATUS DNTX-TFA ENABLE			SYSTEM UP		
RECEIVE STATUS	RB1	RB2	TRAFFIC	RX	TX
TIMING	RFS	BQ	BURST	4	2
BURST	PRB	SRB	SUBBURST	8	8
TRANSMIT STATUS TX CEASE		DELAY 1D7F73			
BTP STATUS					
FOREGROUND BTPO		BACKGROUND BTPO			
BTP CHANGE	READY 11-02-53 01-03-85				
	STATUS				
	COMPLETE 11-03-15 01-03-85				

Figure 4. *TDMA Controller Real-Time Status Display*

Traffic status indicates the number of transmit and receive bursts and sub-bursts. The BTP status displays the BTP number stored in the foreground and background memories and the BTP change status. When a BTP change is complete, the time and date of completion remain on the display until the operator clears it.

The alarm message display tells the operator the type of alarm and the necessary action to be taken, plus the time of occurrence, as shown in Figure 5. The time will remain displayed until the operator clears it because alarm messages from the reference terminal may not be continually transmitted; however, the alarm must be stored to ensure operator recognition.

The following commands are needed at the keyboard for terminal control:

- terminal reset,
- condensed time plan (CTP) down-load (foreground or background memory),
- TFA enable,
- transmit cease, and
- UW miss and high BER measurement enable/disable.

TIME 11:03:33	ALARM DISPLAY	DATE 01-03-85
11:03:30 ---DNTX		---TFA SEQUENCE ERROR
---SYNC LOSS		---RB1 AND RB2 BNQ
---IAP2 LATE		---RTC BTP NO. ERROR
---TFA CDC LOST		---SDNTX PRINCIPAL BURST
---TFA RB BNQ		
---SDNTX MAP		
---HIGH BER MAP		
---UW LOSS MAP		
---LOCAL ALARM		

Figure 5. *TDMA Controller Alarm Display*

Whenever a command is executed, a feedback message from the controller is displayed verifying execution of the command. If the controller fails to respond, the computer will display a time-out and a failure-to-execute message.

All BTP information (except DSI maps which are input at the DSI console) is entered at the operator terminal, including the CTP and the traffic management information needed for routing data to and from the DSI modules. The CTP is normally received by orderwire from the International Operations Center. However, since the COMSAT Laboratories TDMA terminal was designed to be a stand-alone unit, local entry of the CTP was implemented. This feature was found necessary for testing the U.S. Signatory's TDMA terminal where special test CTPs were generated [7]. A special editor was designed to enable easy entry of the CTP in the INTELSAT-specified format. The computer converts this information into a hardware-compatible format and, under operator command, sends it to the TDMA controller. To verify CTP reception, the controller sends the CTP back to the computer where it is compared with the stored CTP. The status display then indicates the BTP number in the appropriate memory—foreground or background. There is also a software time-out for CTP down-load which will display a down-load failure.

The computer stores all status and alarm information on floppy disk. These data are logged in real time, with each event time-tagged to a resolution of 1 s. This permits the operator to keep a history of the TDMA terminal operational status and to track the controller's response to the commands sent from the reference station, which proved useful when evaluating TDMA performance during field testing [5].

If the operator console fails, the TDMA terminal will continue to operate, and terminal control can be executed from the TDMA controller front panel. However, if a BTP change is required, the operator console is needed to generate and down-load the new CTP.

Reference burst generator

The reference burst generator is a special test unit that performs the functions of the primary and secondary reference terminals. It transmits two reference bursts (RB1 and RB2) with the necessary control for acquiring and synchronizing a traffic terminal in either IF, RF, or satellite loop configuration. The unit is capable of receiving the traffic burst, measuring the burst position error, and computing the delay (D_n) sent in the CDC each control frame to the traffic terminal.

Figure 6 is a block diagram of the reference burst generator. The timing circuit establishes the transmit timing, and the burst multiplexer multiplexes the burst data into the 60-Mbit/s P and Q data streams. The carrier and bit timing recovery (CBTR), UWs, and orderwire channels are read from ROM and the SC and CDC messages are generated in the CPU, which uses a Z-80 microprocessor. The receive side of the TDMA controller is used for principal burst A&S. For acquisition, the reference burst generator signals the TDMA controller to enter the search mode. The initial acquisition delay, D_n, is programmed by the operator based on predicted satellite ranging information. Once the TDMA controller receives the principal burst, it measures the burst

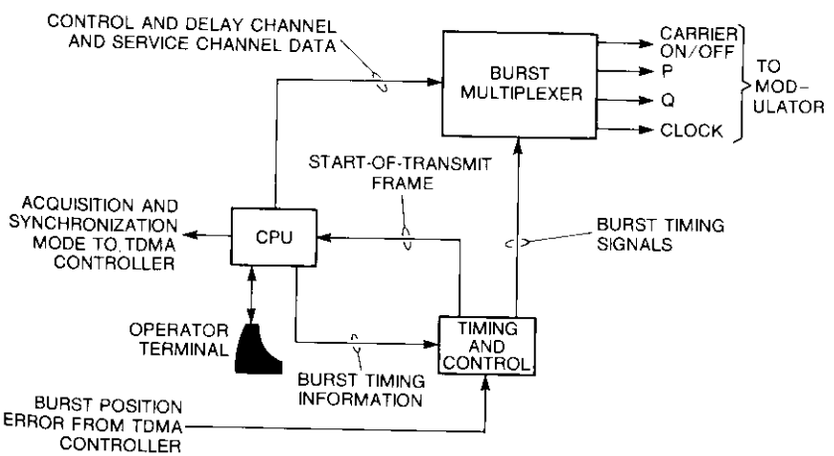


Figure 6. *Reference Burst Generator Block Diagram*

position error and sends it to the reference burst generator where the next D_n number is computed. A new D_n number is calculated and sent to the traffic terminal each control frame, thereby maintaining burst synchronization.

The reference burst generator is controlled by keyboard from a CRT terminal. Figure 7 shows the display for real-time monitoring and control. The SC and CDC are programmable in four modes: immediate, preset, program, and system. The *immediate* mode changes the active status and control codes, while the *preset* mode stores the status and control codes for later execution by operator command. The *program* mode allows a maximum of 60 status and control codes to be sequentially executed or single-stepped under operator control. The *system* commands are used to enable or inhibit automatic Doppler shift and automatic tracking. Automatic Doppler shift, used in IF or RF loop configurations, is implemented by varying the D_n. Automatic tracking enables the reference burst generator to acquire and synchronize the traffic terminal without operator intervention.

REFERENCE STATION	PRESET STATUS	PRESET CONTROL	ACTIVE STATUS	ACTIVE CONTROL	TRANSMIT POSITION
RB1	PRB	IAP1	PRB	DNTX	30208
RB2	SRB	DNTX	SRB	DNTX	31208
BURST TIME PLAN NUMBER = 00000			TERMINAL Dn NUMBER = 3866624		
AUTOMATIC DOPPLER SHIFT = OFF			AUTOMATIC TRACKING = ON		

ENTER SYSTEM CHANGE MODE

F1 - IMMEDIATE F3 - PROGRAM

F2 - PRESET F4 - SYSTEM

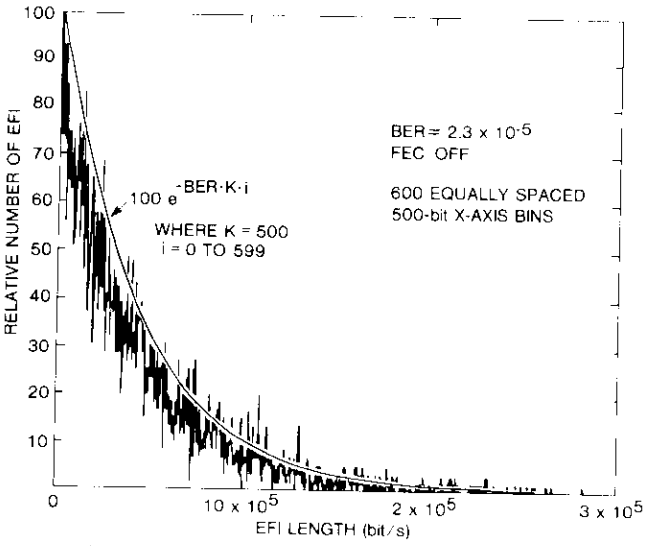
F5 - HELP

Figure 7. *Reference Burst Generator Real-Time Monitor and Control Display*

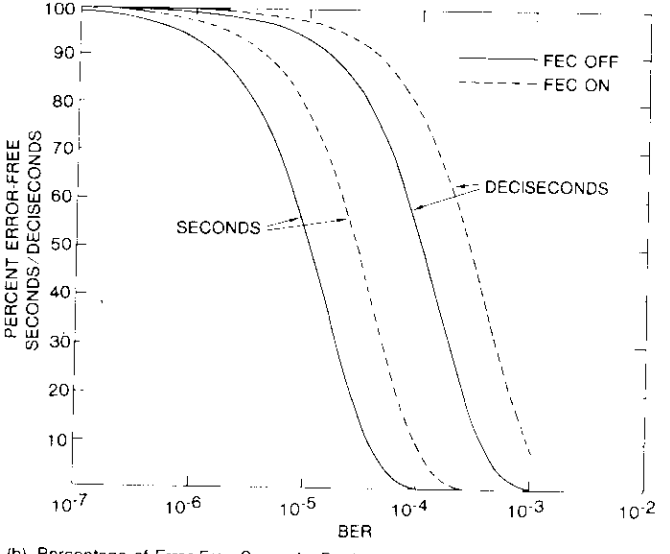
This reference burst generator, used in the field test operating in satellite loop [5], is essential for verifying the TDMA controller A&S operation. It also enables loop configurations for baseband testing of the DSI/DNI modules.

BER/EFI measurement unit

The BER/EFI unit measures performance in the TDMA traffic channel on $N \times 64$-kbit/s traffic channels ($N = 1$ to 128, as selected by the operator) and records the results on floppy disk for later analysis by the PDP 11-04 computer. This unit was used in the TDMA field test [5]. Figure 8 shows EFI distribution and an error-free seconds plot obtained during field tests.



(a) EFI Distribution on a 64-kbit/s Satellite Channel Without FEC



(b) Percentage of Error-Free Seconds/Deciseconds vs BER With and Without FEC

Figure 8. *EFI and EFS Plots*

BER and EFI measurements were made by transmitting a pseudonoise (PN) sequence through the TDMA system and recording the distance between the bit errors in terms of bit clock periods. After each test period, the EFI interval measurement was processed to provide error-free seconds and EFI histograms. The BER and EFI measurements were made by interfacing a commercial BER test set to a standard port on the DSI interface and looping the transmitted PN sequence through the TDMA system to the BER test set receiver. An EFI unit was built to operate with the commercial BER test set. The BER test set provided a pulse for each bit error in the received PN sequence, and the EFI unit counted the number of clock cycles between each bit error pulse and loaded this count into memory. The memory has capacity for 64K addresses, each able to accept 2^{16} bits. If the interval between bit errors exceeded this count, a flag bit was set indicating the interval to be greater than 2^{16} bits.

Equipment configuration

Figure 9 is a photograph of the COMSAT Laboratories TDMA traffic terminal (less DSI modules). The terminal is housed in two standard 19-in. bays approximately 8 ft in height, one bay for the TDMA controller and modem, and one bay for the computer, reference burst generator, BER/EFI

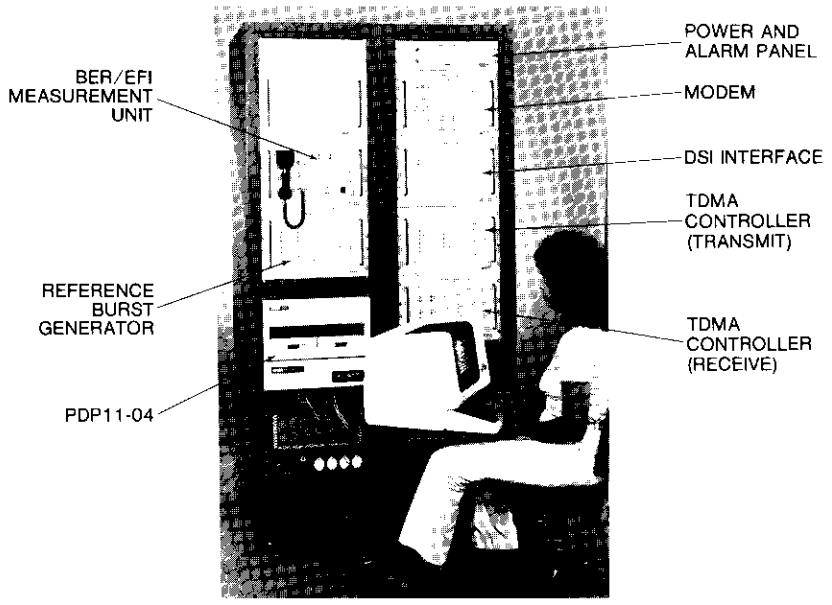


Figure 9. *COMSAT Laboratories 120-Mbit/s TDMA Traffic Terminal*

measurement unit, and VOW unit. All circuits are implemented on wirewrap cards with differential emitter-coupled logic (ECL) interfaces between cards. This eliminates the possibility of timing problems, especially when using extender cards.

LED displays and test points are identified in Table 4. The traffic terminal provides monitor indicators for visual verification of terminal A&S status. The terminal responds to A&S control directives from either reference burst 1

TABLE 4. TRAFFIC TERMINAL DISPLAY AND TEST POINTS

FUNCTION	TEST POINTS	MONITOR POINTS (LEDs)
MODEM	*Modulator* *P* and *Q* data, clock, eye pattern, modulator output *Demodulator* *P* and *Q* data (unsampled), *P* and *Q* sampling clocks, *P* and *Q* data (sampled), recovered carrier, clock	*P* and *Q* data, clock, +5 V, −5 V, +15 V, −15 V
TDMA RECEIVE	*P* and *Q* data, SORMF, SORF, UW detect, aperture, FEC on/off, RB1W and RB2W (timing signals)	*RB1 and RB2 A&S* SMA, GMA, BA, BTA, INOP, SRB, PRB, BQ, RFS
TDMA TRANSMIT	*P* and *Q* data, clock, SOTMF, SOTF, carrier on/off, FEC on/off	*BTP Change* Load, echo verified, ready, complete, fail *Control Status* IAP1, IAP2, SYNC, DNTX, SDNTX
DSI INTERFACE	Tx 2.048-MHz clock, Tx frame, Tx window, Tx 16.384-MHz clock, Rx 15-MHz clock, Rx frame, Rx burst start, Rx 16.384-MHz clock, Rx enable	*Synthesizer* Symbol clock, Tx DSI clock, Rx DSI clock
REFERENCE BURST GENERATOR	*Transmit* Clock, SOTMF, SOTF, *P* and *Q* data, carrier on/off	*Reference Burst* IAP1, IAP2, SYNC, DNTX, INOP, SRB, PRB
REFERENCE BURST GENERATOR	*Receive* Clock, SORMF, SORF, UW3, aperture, window, *P* and *Q* data, carrier on/off	*Traffic Burst Synchronization* Auto, manual

(LED labeled RB1) or reference burst 2 (RB2). The terminal is programmed to progress through the following series of receive acquisition steps: search mode acquisition (SMA), gated mode acquisition (GMA), burst acquired (BA), burst timing acquired (BTA), burst qualified (BQ), and RFS. In addition, during the receive frame acquisition process, the terminal will establish whether RB1 or RB2 is the primary reference burst (PRB) and which RB is the secondary reference burst (SRB). A reference burst may also declare itself inoperative (INOP).

The transmit frame acquisition process also requires the terminal to progress through a series of steps before it becomes synchronized with the TDMA frame. The transmit frame acquisition steps are as follows: initial acquisition, phase 1 (IAP1); initial acquisition, phase 2 (IAP2); and TFS (SYNC). The terminal also provides indicators for the DNTX and SDNTX commands. Each of the above indicators is repeated for PRB and SRB control status.

Critical design issues

The speed of operation, especially in regard to the UW detector and the FEC unit, was a critical item in the TDMA traffic terminal design. The design of the DSI speech detector was critical because its performance influences speech quality. Other important considerations were the interfacing of 32 DSI modules to the TDMA controller, and the design of a receive-side retiming unit with a demodulator interface which required no clocks after the last symbol of data.

UW detector

The purpose of the UW detector is to identify the unique bit pattern located in the preamble of each received TDMA burst. When the pattern is located, a correlation pulse is generated which synchronizes the receive hardware to the incoming data stream, allowing demultiplexing of the data channels from the burst structure. The implementation of a UW correlator that would operate reliably at the 60-MHz symbol rate using the recovered clock from the demodulator was critical. At this clock rate, UW timing becomes very sensitive to the duty cycle and phase jitter present on the recovered clock.

Three design architectures were considered: an analog approach, a digital approach utilizing exclusive-OR correlation, and a digital approach utilizing programmable read-only memory (PROM) correlation. The first two approaches were eliminated because of hardware complexity and circuit size. The PROM correlation technique design was simple, flexible, and required less hardware. However, the 60-MHz clock rate was too high for the rated propagation times for currently available PROMs. This left two available design options. The first was to artificially increase the clock period of the recovered clocks by passing them through a delay circuit. This approach was considered unacceptable because the delay could vary with time, temperature, environment, and manufacturer tolerances, negatively affecting the performance of the UW detector or causing failure. Also, this would require that the UW detector be calibrated either on a regular basis or at least whenever a new UW detector was placed into service.

The second option was to demultiplex the input 60.416-Mbit/s data stream into two data streams of 30.208 Mbit/s each. At this rate, the ECL PROMs had excess propagation delay margin and the data could be handled in a synchronous digital manner without the need for special delay devices, allowing the UW detector to be replaced without adjustment of any kind, regardless of aging, temperature, environment, and manufacturer's integrated circuit (IC) tolerances. However, this caused the number of ICs in the correlator portion of the UW detector to double.

The UW detector logic performance in the presence of phase jitter and duty cycle variations on the recovered clock presented another design problem. Setup times and hold times on various ICs could be violated by either the positive or negative portion of the clock's period shrinking or expanding on a clock-by-clock basis. To eliminate this problem, the UW detector was designed to operate only on the leading edge of the incoming recovered clock. Therefore, by using the leading edge transitions for clocking sequences, the fluctuations in the clock duty cycle would not cause problems in the UW detector. Developing the UW detector with this approach allowed the COMSAT Laboratories TDMA to be more tolerant of demodulator clock instabilities.

Retiming unit

In the TDMA terminal, the retiming function transfers the alignment of the data from the demodulator burst clock to the continuous terminal clock. Retiming is necessary because the demodulator clock changes phase on a burst-by-burst basis and dissipates at the end-of-burst reception. The retiming unit provides a continuous clock to the demultiplexer and terrestrial interfaces.

The critical design issue in the retiming unit is the possibility of losing data at the end of a burst due to the delay inherent in the UW detector. Data can be lost if the recovered clock decays or changes phase before the last symbol of data in the burst has been clocked through the UW detector and into the retiming unit. This could be crucial for receiving reference bursts which have the CDC in the last portion of the burst. To avoid this problem and to guarantee that the COMSAT Laboratories TDMA terminal would work with any modem, the design causes the last symbol of data to be clocked directly into the retiming unit by the last symbol clock from the demodulator. This eliminates the need for additional clocks after the last symbol of data.

The block diagram in Figure 10 depicts the implementation of the retiming unit. The UW detect signal resets the retiming circuit prior to retiming the received data. Both the delayed data from the UW detector (P_d, Q_d) and the data from the demodulator (P_m, Q_m) are retimed. After retiming, the data from the demodulator are delayed 16 clock cycles through a shift register, thereby aligning both data paths (P_m, Q_m, and P_d, Q_d) at the input of the multiplexer. The multiplexer selects the retiming unit's shift register data path 16 clock intervals after UW detection. Thus, data are clocked directly from the modem into the retiming circuit.

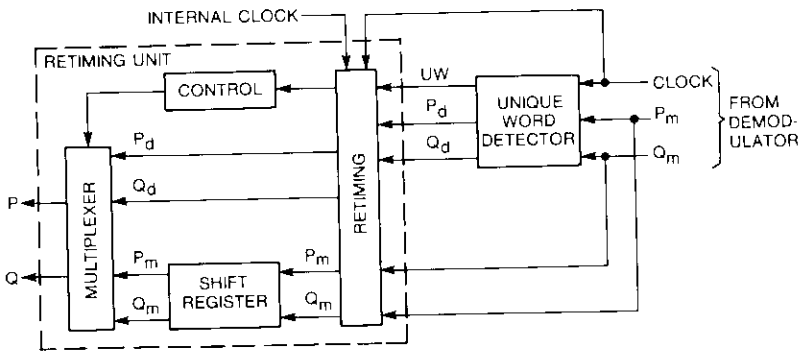


Figure 10. *Retiming Unit Block Diagram*

INTELSAT later modified the carrier and bit timing sequence to make the first 48 symbols of the CBTR sequence pure carrier (*i.e.*, all 1's). As a result, the clock recovery circuit is unaffected by the CBTR sequence of a trailing burst for at least 48 symbols.

Forward error detection

The FEC in the INTELSAT 120-Mbit/s TDMA is a (128,112) block code which is selectively applied on a burst-by-burst basis. The design issue was whether to implement the FEC in serial or in parallel form. A serial design must work at 120-Mbit/s clock rate, requiring ECL and very sensitive timing constraints. Because of this, an 8-bit (15-MHz) parallel approach was chosen, eliminating the high-speed clocks and allowing a simpler, fully synchronous hardware implementation. The parallel design method developed for implementing the INTELSAT block code is described in Reference 8.

DSI interface

In the DSI interface, the design goal was to develop a technique for busing the traffic data between the DSI modules and the TDMA controller. Key influencing elements were the maximum number of DSI modules (32), equipment redundancy, and the physical spacing of the DSI modules and the TDMA controller.

Numerous interface approaches were studied, including bidirectional buses, serial unidirectional buses, and individual unidirectional buses. The bidirectional buses were eliminated because the task of coordinating the transmit and receive data transmissions on the same bus was too complex. This complexity was further compounded by the fact that the transmit and receive TDMA frames are asynchronous due to satellite Doppler and the difference in the transmit and receive BTP change implementation.

The serial unidirectional bus connects all DSI modules to the TDMA controller using a single bus for transmit and a single bus for receive. This approach was eliminated primarily because of the daisy chain connections required to interface 32 DSI modules. Whenever a DSI module is powered down (*e.g.*, for maintenance) or a new DSI module is added, it must not affect the bus.

The individual unidirectional bus approach was selected: one bus for the transmit interface and one bus for the receive interface. The transmit-side data (DSI to TDMA) were transferred at a 2.048-MHz clock rate, 8 bits parallel. This allowed the data to be transferred from each DSI (one sub-burst, 128 satellite channels, and 2,048 bytes) in 1 ms, giving a transfer guard time from each DSI to the TDMA of one-half a frame period. The data are stored in a buffer and transmitted in the TDMA burst on the next frame at the time prescribed by the BTP. The receive-side data (TDMA to DSI) are transferred directly to the DSI module at a 15-MHz clock rate, 8 bits parallel, with no buffering.

This approach offered the least risk to existing data transmission whenever a DSI module was powered down or a new one added to the system because each DSI is connected with a separate set of cables (transmit and receive side). The combination of separate interface ports and buffers in the TDMA controller for each DSI interface and the 8-bit parallel transfer eliminated concerns over placement of DSI units within the earth station. However, this control simplicity and system layout flexibility increased the quantity of interface hardware, cabling, and connectors.

DSI speech detector

The performance of the speech detector in the DSI module is a critical issue because it influences the quality of the channel. If the speech detector

does not work properly, the user may notice clipping at the beginning or end of speech and dropouts during speech. This phenomenon is dependent upon the relationship between the speech and noise levels in the channel. Since these levels are both variable, a variable-threshold type of speech detector [4] was designed for the DSI module. The threshold adapts to changes in the noise level, thereby optimizing the detection of speech with respect to the existing noise level. The performance of the adaptive-threshold speech detector proved superior to that of fixed-threshold speech detectors. As a result, an adaptive speech detector was specified for the U.S. Signatory's TDMA traffic terminals.

Conclusions

COMSAT Laboratories development of an experimental prototype terminal has provided the means for testing network control protocols against a working implementation. Because the terminal was implemented by a team of engineers that had not assisted in writing the TDMA specification, their interpretation of the specification provided important feedback to INTELSAT, which often asked for clarification on implementation issues raised by various manufacturers.

The design engineers helped the U.S. Signatory prepare an equipment specification for operational service, and provided continuing support during the development, installation, and testing of the terminal. The need for many of the operational features was recognized during the implementation of the laboratory terminal, and these features, along with methods of implementation, were often discussed and used by the operational equipment manufacturer.

The installation and operation of the TDMA terminal at an earth station involves connection to RF equipment that is properly aligned and equalized for wideband digitally modulated carriers. The laboratory terminal was field tested at the Andover, Maine, earth station to confirm link equalization procedures, as well as to confirm the TDMA A&S performance of the new network control protocols. This early field test demonstrated that the A&S and link BER objectives would be met by operational TDMA equipment. In addition, the laboratory terminal was used in verification testing of the operational TDMA equipment at the Etam, West Virginia, earth station [7].

The equipment operated well in stand-alone configuration, and was used to measure A&S performance and to make BER and EFI data measurements on TDMA traffic channels. The hardware design proved to be extremely rugged and reliable, and the parallel implementation of the FEC codec was clearly demonstrated. The design for the fully synchronous UW detector operated as hoped, and is an important achievement for high-speed digital correlators.

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Robert P. Ridings received a B.S.E.T. degree from the Capitol Institute of Technology in 1969, and a B.S.E.E. and M.S.E.E. from George Washington University in 1973 and 1979, respectively. He joined COMSAT Laboratories in 1970, and is currently a Senior Scientist in the Network Technology Division working on the Advanced Communications Technology Satellite (ACTS) TDMA ground segment. Prior to this, he was responsible for the design of digital speech interpolation systems and TDMA systems. He was Program Manager for the development and testing of the COMSAT experimental TDMA traffic terminal and the reference station emulator, and was Test Manager for the COMSAT MP2 TDMA traffic terminal located at the Etam, West Virginia, earth station.

Richard R. Lindstrom received a B.S.E.E. from the University of Illinois, Urbana-Champaign, in 1975, and an M.S.E.E. from the Johns Hopkins University in 1979. He joined COMSAT Laboratories in 1979, and is currently Manager of the ACTS TDMA Department of the Network Technology Division, where he is supervising the development of NASA Ground Station TDMA equipment. From 1983 to 1985, he was Manager of the Network Engineering Department of the Network Technology Division, helping to develop networking concepts and supervising the development of networking equipment. Prior to this, he worked on projects involving the development and field trial of various TDMA designs. Mr. Lindstrom is a member of IEEE, Tau Beta Pi, and Eta Kappa Nu.

Thomas R. Dobyns received a B.S.E.E. from the University of Florida in 1963, and an M.S.E.E. from George Washington University in 1968. He is presently Associate Director of the Network Technology Division at COMSAT Laboratories, where he is responsible for supervising the TDMA network control and TDMA earth terminal design activities for the NASA Advanced Communications Technology Satellite (ACTS) Program. His experience includes TDMA systems and terminal design, onboard baseband processing, and data networking. Mr. Dobyns is a member of IEEE.

Index: coding; communication satellites; modulation, demodulation, modems; time division multiple access; transmission

120-Mbit/s TDMA modem and FEC codec performance*

C. J. WOLEJSZA, JR., J. S. SNYDER, AND J. M. KAPPES

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Abstract

Introduction of the INTELSAT time-division multiple-access (TDMA) system into commercial service was preceded by a substantial amount of research and development, particularly for the modems and forward error correction (FEC) codecs required for TDMA operation. The modems are subject to significant compromises between the need for rapid acquisition, robust tracking, and operation in a nonlinear channel. In addition, the performance of the FEC codec is closely related to that of the modem and requires considerable attention to its place in the TDMA system architecture. This paper reviews these operational requirements and presents the results of modem and codec performance measurements which demonstrate the feasibility of meeting INTELSAT specifications.

Introduction

Initially, time-division multiple-access (TDMA) studies were undertaken to determine how to achieve maximum efficiency from satellite transponders [1]–[3]. In TDMA, only one earth station carrier is present in a satellite transponder at any given time, so that the transponder must time-share to

*This paper is based on work performed at COMSAT Laboratories under the sponsorship of the International Telecommunications Satellite Corporation (INTELSAT). Views expressed are not necessarily those of INTELSAT.

achieve access to several earth stations. This operating mode places several constraints upon system modems and codecs. Since each demodulator receives coherent phase-shift keying (PSK) signals in burst mode from a number of transmitters, the best compromise between satellite bandwidth and power must be sought. Furthermore, for overall efficiency, the time required for demodulator synchronization must be minimized and the maximum power of the satellite transponder must be used.

With only one carrier present at any given time, the transponder transmission capacity is limited by the performance of the modulation/coding scheme in a band-limited and nonlinear environment rather than by intermodulation distortion for the current frequency-division multiple-access (FDMA) FM systems. Operational TDMA networks require equalization of the transmission links with several transmit paths and one receive path.

The use of coding requires the modem to function at lower signal-to-noise (S/N) ratios than would otherwise be the case, so the overhead allocated for forward error correction (FEC) must be minimized. The use of the INTELSAT TDMA network for data as well as voice traffic requires a considerably higher degree of robustness in the modem than that previously obtained in experimental systems [4]–[6]. Of particular concern is the performance of the synchronization circuits in a nonlinear environment at low S/N ratios [1].

The first section of the paper summarizes the INTELSAT modem and codec performance requirements and outlines their working environment. The configuration and design issues for the modem built by COMSAT Laboratories are discussed, including the design and implementation at the FEC codec, the coding scheme specified by INTELSAT, and the measured performance.

Finally, two transmission sequences for system testing the modems will be given. These tests included system alignment and equalization, bit error rate (BER) performance for both 72-MHz and 77-MHz INTELSAT V transponders as a function of nonlinear operating condition, adjacent channel interference, and sensitivity of the modem to perturbations in link equalization.

Modem performance requirements

Four fundamental parameters define the modem performance: BER, the probability of missing the burst, and the probability of cycle slipping in either the recovered carrier or the recovered clock. The required BER for the INTELSAT TDMA system is a compromise between achievable BER in the nonlinear operating environment and the available capacity in terms of satellite transponder power and bandwidth [3]. INTELSAT has specified the characteristics of modem transmit spectral shaping and the operating characteristics

of each of the principal nonlinearities in the transmission channel and of the principal filters, especially the satellite input and output multiplexer filters [7], [8]. The BER performance is recommended for all stations, but for the reference station is specified at defined operating points of the nonlinear amplifiers.

The probability of missing the burst is unique to the TDMA environment and difficult to define in terms of only the modem. The amount of synchronization time which must be allocated at the beginning of every burst (preamble time) must be long enough to permit synchronization to occur before data can be received, but short enough to maintain a reasonable frame efficiency. Modem synchronization circuit transient behavior alone is inadequate to define modem acquisition [4]. Consequently, INTELSAT evaluates acquisition based upon overall synchronization performance on which the TDMA network obtains and maintains a precise time reference by the insertion of a unique word in the burst at the end of the synchronization preamble to properly demultiplex the received data.

In satellite systems, synchronization is complicated by satellite motion and clock drift among the transmission sources, causing the relative positions of the bursts to change with time, and hence the synchronization process must be constantly updated. The unique word has carefully designed autocorrelation properties to maximize the probability of correlation detection at the correct time and minimize the probability of false detection at the incorrect time [9].

Statistically well-defined, the probability of false detection is affected by the preamble BER. During normal synchronized operation, the TDMA controller generates an aperture which recognizes correlation peaks only in that portion of the TDMA frame close to the true location of the unique word. However, during acquisition no aperture can be used, so poor modem acquisition performance degrades the probability of detecting the true unique word. Prior experience [4], [10] has indicated that phase-locked loop techniques tend to hang up during acquisition, significantly increasing the probability of missing the true correlation peak of the unique word. In order to avoid potential problems with phase-locked modem implementation, INTELSAT has adopted specifications for the probability of unique word miss based upon the performance of modems using carrier and clock recovery techniques without phase-locked loops.

Carrier and clock cycle slipping place constraints upon the modem which are antithetical to those required for rapid acquisition. The INTELSAT TDMA system uses direct, nondifferential bit encoding so proper data recovery and FEC decoding are sensitive to changes in carrier phase caused by carrier slips and to timing offsets caused by clock slips. The requirements for cycle slipping performance are quite stringent and have resulted in a set of

specifications with a relatively long preamble. The important INTELSAT TDMA modem specifications are summarized in Table 1.

TABLE 1. SUMMARY OF INTELSAT V TDMA SPECIFICATIONS

BER (uncoded)	5×10^{-3} at E_b/N_o = 6.3 dB
Linear Channel	1×10^{-4} at E_b/N_o = 10.0 dB
	1×10^{-6} at E_b/N_o = 12.6 dB
	1×10^{-7} at E_b/N_o = 14.0 dB
BER (uncoded)	5×10^{-3} at E_b/N_o = 7.0 dB
Nonlinear Channel	1×10^{-4} at E_b/N_o = 11.0 dB
HPA at 10-dB Input Backoff	1×10^{-6} at E_b/N_o = 14.0 dB
TWT at 2-dB Input Backoff	
Probability of Unique Word Miss	1×10^{-8} at E_b/N_o = 7.0 dB
Probability of Carrier Cycle Slip	1×10^{-4} at E_b/N_o = 7.0 dB
Probability of Clock Cycle Slip	1×10^{-5} at E_b/N_o = 7.0 dB
Bit Rate	120 Mbit/s
Channel Filter	40-percent square-root raised cosine
Preamble Time	176 symbols
Burst-to-Burst Level Variation	5 dB
Nominal Bandwidth	72 MHz

TDMA modem design

The TDMA modulator shown in Figure 1 uses two parallel data paths in a conventional design. The interface outputs drive two identical low-pass filters to provide the spectral shaping of the data prior to transmission. The filter outputs provide baseband waveforms to two double-balanced mixers driven by the in-phase and quadrature components of the carrier oscillator provided by the in-phase and quadrature hybrid. The mixer outputs are summed, amplified, and filtered to remove spurious out-of-band signals prior to the final output. The burst on/off control is exercised by means of an IF switch between the transmit oscillator and the quadrature hybrid.

Transmit filters for spectral shaping

The significant design issue for the modulator is the implementation of the transmit filters for spectral shaping. The INTELSAT specifications require a square root Nyquist filter with a 40-percent rolloff factor and equalization to compensate for the sin x/x characteristics of the non-return-to-zero data. Low-pass filtering achieves spectrum symmetry which is necessary to fit the

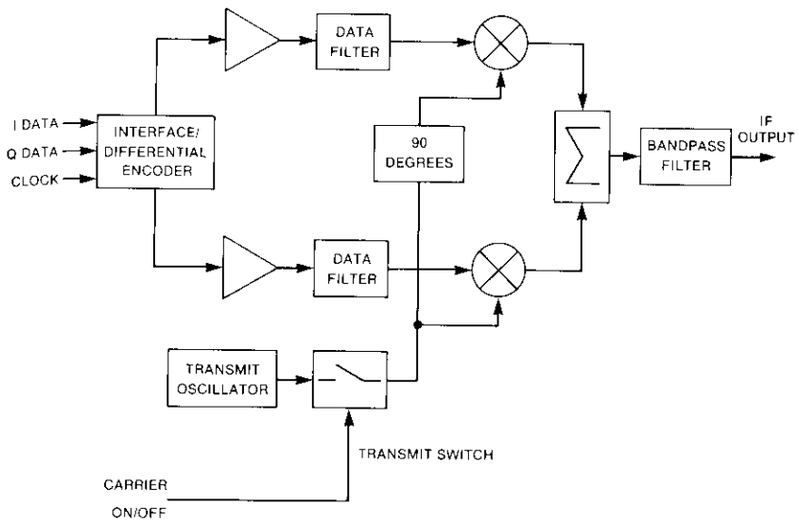


Figure 1. *TDMA Modulator Functional Block Diagram*

required spectral mask, minimizes crosstalk between the in-phase and quadrature channels, and eliminates aliasing. The x/sin x equalization was built into the filter design, resulting in a relatively compact implementation. Measured and specified transmit filter performance (magnitude and group delay) is shown in Figure 2.

Burst demodulator configuration

The burst demodulator block diagram shown in Figure 3 incorporates a number of novel features. The receive IF signal is first passed through a transversal equalizer, permitting fine tuning of the overall system transfer function by acting in the time domain to reduce the intersymbol interference. The equalized signal is brought to a constant level by the automatic gain control (AGC) amplifier which, by a careful choice of the gain controlling element and parameters, permits very fast transient times, allowing the amplifier to respond to each burst individually.

The actual demodulation process is accomplished by reversing the operations performed by the modulator. The output of the AGC amplifier is fed to two mixers with local oscillator inputs driven in quadrature by the recovered carrier via a quadrature hybrid. Dual low-pass filters similar to the transmit filter implementation provide the receiver matched filtering as well as rejection of the harmonics of the carrier. Dual limiters and samplers operating from

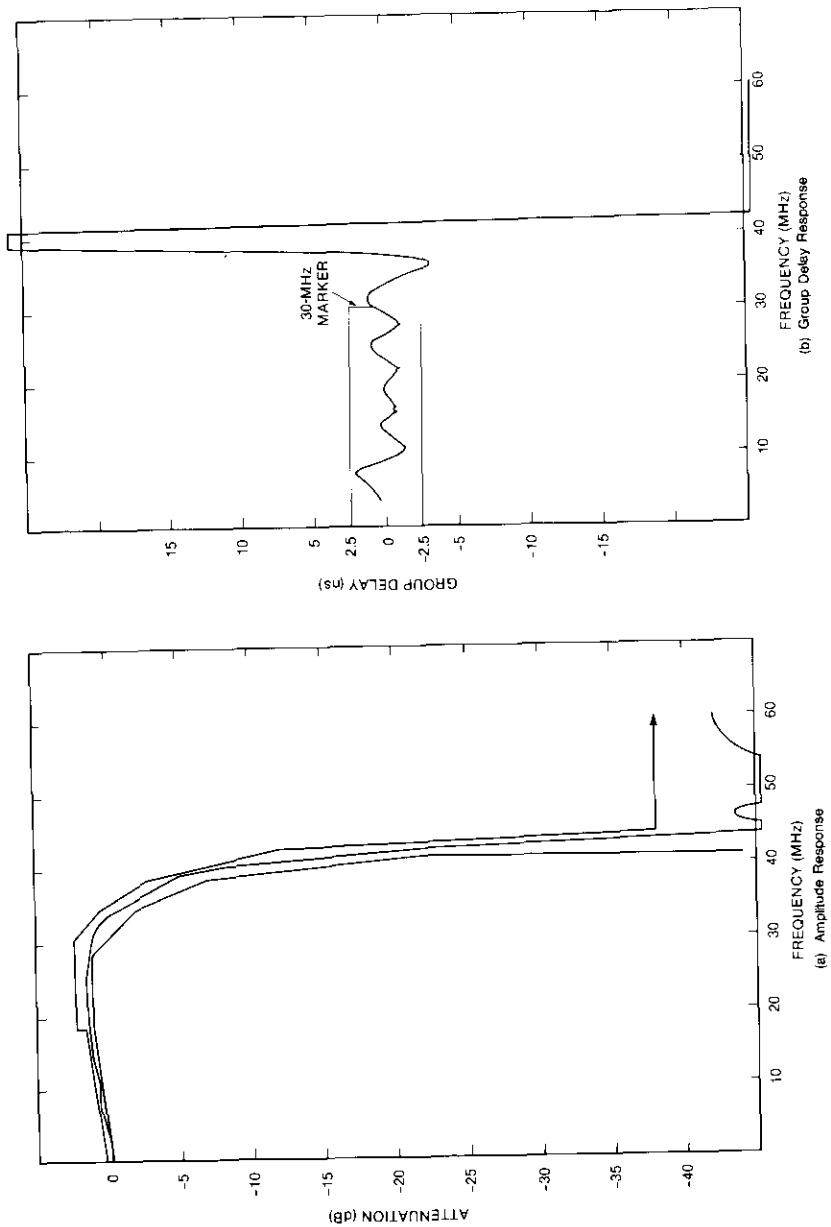


Figure 2. *Transmit Filter Characteristics*

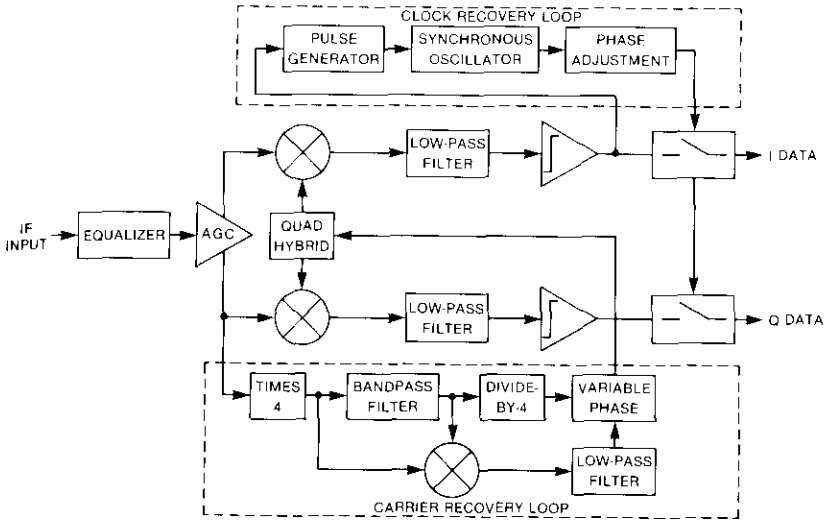


Figure 3. *TDMA Demodulator*

the recovered clock provide the output data, also in parallel format. The combination of transmit and receive filter responses yields an overall Nyquist pulse shape with significantly reduced intersymbol interference and a noise bandwidth approximately equal to the Nyquist bandwidth. The transfer functions of the receive filter are compared to the specifications in Figure 4.

Feed-forward carrier recovery configuration

In the carrier recovery operation, the carrier phase information is extracted from the modulated signal by frequency multiplication by four. A narrow bandpass filter provides long-term averaging and improvement in *S/N* ratio. Frequency division by four restores the carrier frequency to its original value for use in the demodulator. With this method, any frequency offset present in the input signal due to satellite oscillator offset and other causes is multiplied by four, causing a considerable phase shift after the bandpass filter, which in turn can cause significant BER degradation for the frequency offsets experienced in satellite systems (± 25 kHz).

The conventional approach to this problem has been to frequency translate the reconstructed carrier to another IF frequency prior to filtering, retranslate the recovered carrier back to the correct frequency, and control the phase shift of the filter by adjusting the frequency of the translation oscillator [1].

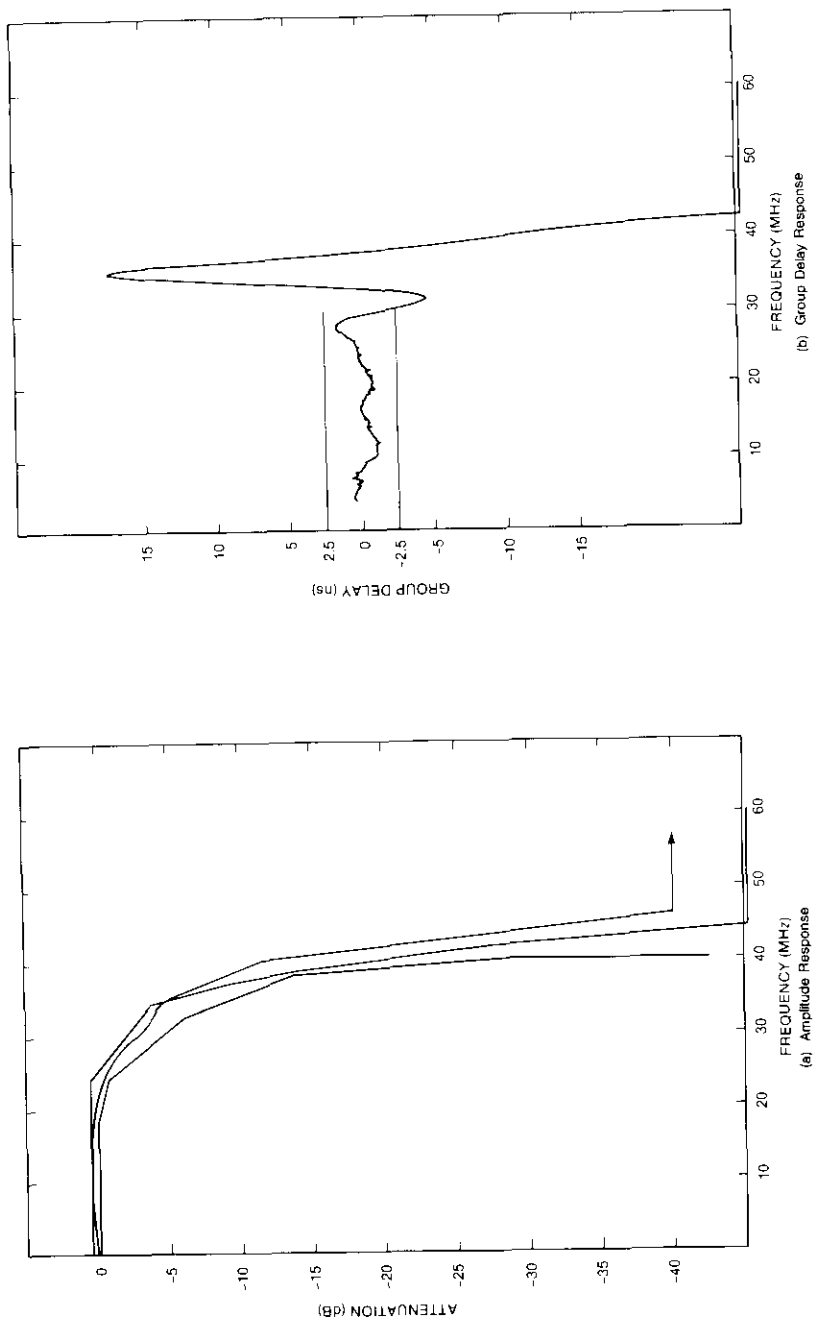


Figure 4. *Receive Filter Characteristics*

This requires a voltage-controlled oscillator (VCO), another frequency multiplication by four for the VCO output, two mixers, and an output filter.

Alternatively, a feed-forward technique is employed. The phase shift caused by the filter is measured in the same way as in the conventional approach by comparing the phases of the input and output of the filter. The output of the phase comparator is averaged by a low-pass filter and passed to a voltage-variable phase shifter at the output of the divide-by-four circuit. By appropriate selection of the low-pass filter time constant and the gain of the combination of voltage-variable phase shifter and filter, the phase variation of the carrier recovery filter is balanced by the phase shift of the voltage-variable phase shifter. Thus, the overall phase shift of the carrier recovery loop can be held constant over a wide range of frequency offsets.

Clock recovery by synchronous oscillator

The clock recovery is also accomplished with an unconventional approach. Clock information is extracted from the hard-limited data by a pulse generator circuit which produces a pulse for every zero crossing. The clock information contained in the pulse train is filtered by an injection locked "synchronous" oscillator [11]. This circuit consists essentially of an oscillator operating at the nominal symbol rate, with the input pulse train coupled into the oscillator feedback path. After an initial transient, the oscillator will acquire the frequency and phase of the driving signal and thereby track it. The high Q of the oscillator circuit provides noise rejection and a clean recovered clock is obtained.

An adjustable phase shifter allows optimization of the sampling time at the data detectors, thus providing the output clock. In contrast to the conventional bandpass filter approach in which the receive clock vanishes at the end of every burst, the receive clock is always available, even in the absence of bursts.

Modem design for noise performance

Two factors must be considered in the circuit design for carrier recovery using the multiplication method: the effect of the data modulation on the carrier or pattern noise, and the effect of nonlinearities on thermal noise. Pattern noise is not generally considered because PSK nominally yields a constant amplitude signal which does not affect the fourth power device output. However, in the bandlimited channels usually encountered in both satellite and terrestrial systems, band limiting introduces a significant amount of amplitude variation at phase transitions which is magnified by multiplication by four. Thus the regenerated carrier is degraded.

Effects [1] of pattern noise include a 2- to 3-dB loss in carrier power and the generation of a fixed-noise floor with a power spectral density comparable to that resulting from thermal noise at moderate (10 to 15 dB) *S/N* ratios. Lindsey and Simon [12] have developed a general relationship for the degradation in *S/N* ratio of an *M*th-order nonlinear device which reduces to the following for $M = 4$ quadrature PSK (QPSK):

$$S/N = \frac{a}{16(1 + 3/a + 135/a^2 + 208/a^3)} \tag{1}$$

where a = carrier-to-noise $(C/N)_i$, input *S/N* ratio
S/N = output *S/N* ratio.

Figure 5 illustrates this relationship and shows that the frequency multiplication-by-four operation results in a loss in *S/N* ratio of at least 12 dB, which worsens rapidly below an input *S/N* ratio of 12 dB due to noise mixing with itself in the nonlinearity. After the filtering, the original carrier frequency is restored by frequency division by four, which improves the *rms* phase

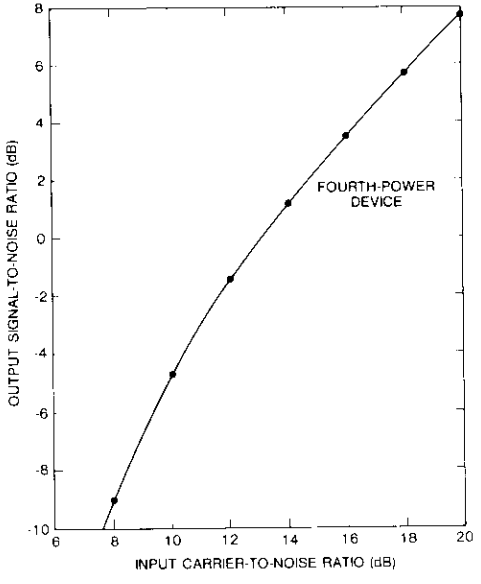


Figure 5. *Signal-to-Noise Ratio for Fourth Power Device*

jitter by 12 dB. However, at moderate to poor *S/N* ratios at the divider input, the divider will miscount the input, producing a phenomenon equivalent to the cycle skipping of a phase-locked loop.

The carrier tracking circuit is characterized by an equivalent noise bandwidth, B_n, which, together with the equivalent *S/N* ratio at the carrier filter input, determines the *rms* phase jitter of the recovered phase relative to the input phase. In general,

$$\sigma_0^2 = \frac{B_n}{B_i(S/N_i)} \tag{2}$$

where S/N_i is the *S/N* ratio at the tracker input in bandwidth B_i.

The frequency multiplication method of carrier recovery for *PSK* produces an excessive degradation in *S/N* ratio that is not removed by the division operation. For example, consider the fourth power device curve shown in Figure 5 at a typical input *C/N* ratio of 12 dB. The output *S/N* ratio is -1.4 dB, which after the frequency division by four, is improved by 12 dB to 10.6 dB, resulting in a net loss of 1.4 dB. The impact of phase noise on the BER is shown to be minor by the measured performance below.

Carrier cycle skipping

The carrier recovered from the modulated signal can have one of four phases (0, $\pi/2$, π, or $3\pi/2$) relative to the true carrier, resulting in phase ambiguity [13]. A cycle skip can cause a shift in recovered carrier phase, resulting in three chances out of four that the carrier phase will be wrong. This effect can be eliminated by differentially coding the information in terms of data transitions because errors in the output data always occur in pairs since each channel bit error affects two data bits.

When FEC coding is used, as in the INTELSAT V TDMA system, these paired errors produced by the differential decoder will degrade the performance of the FEC decoder. Consequently, differential coding is not used and ambiguity is resolved in the INTELSAT modem by using the unique word. However, any subsequent cycle skip in the recovered carrier changes the ambiguity state of the carrier and therefore can scramble the remaining data. Clearly, the designer must exercise great care in selecting system parameters to minimize this effect. The cycle-skipping performance of the bandpass filter can be estimated using a modification of Rice's click theory [14] for frequency modulation (FM). The cycle skipping performance of conventional phase-locked loops provides a guide for carrier tracking design.

The application of Rice's click theory is based upon the assumption that the input to the carrier tracking filter is the sum of a sinusoidal signal with band-limited Gaussian noise. Though not strictly Gaussian with the pattern noise component, the thermal component of the noise is usually much larger than the pattern noise, dominating the characteristics of the composite signal. Rice has calculated the probability that the combined vector sum of signal and noise will encircle the origin and therefore cause an FM click, which is precisely the same effect which causes a cycle skip or miscount of the divider in a carrier-tracking loop. For QPSK and a single-pole carrier recovery filter, the occurrence of this event can be approximated by

$$N = \sqrt{f_c B_i / \pi}\ \text{erfc}\ (\sqrt{r_0}) \qquad (3)$$

where N = number of events per second
f_c = cutoff frequency of the filter (3 dB)
B_i = input noise bandwidth
r_0 = S/N rate at filter output.

Initial carrier acquisition

To quickly reduce cycle skipping, the designer is faced with a compromise between minimizing steady-state jitter, which requires a narrow loop bandwidth, and the need to establish phase synchronization, which requires a wide loop bandwidth. For the bandpass filter technique, a linear circuit is used to analyze transients in the carrier recovery circuit if superposition is applicable.

Acquisition performance of the bandpass filter circuit is greatly affected by the previous carrier burst signal which must decay to a small value while a new arrival burst signal builds up. Single-pole filters are normally used because of their simplicity. The envelope of the decaying signal falls exponentially, while that from the new arrival signal grows asymptotically to the steady-state value with the same time constant. The resulting transition can be obtained by superposition. Since the frequency offsets between the old and new bursts at the filter are usually kept small, it is sufficient to determine the transient response for an initial, unknown phase difference. There may also be amplitude and guard time differences between the new and old bursts.

A TDMA carrier recovery design based on the INTELSAT V system parameters has been described [1]. This design indicated that a 400-kHz filter bandwidth would provide a maximum S/N ratio for a 176-symbol preamble, have a steady-state S/N ratio of about 14 dB, and have a corresponding cycle skipping frequency of 4 in 10^6 s.

Measured modem performance

Actual measurements confirmed that performance goals specified by INTELSAT were achieved. As noted above, four basic performance parameters need to be examined. The measured BER for the modem alone, operating back-to-back with additive white Gaussian noise, is shown in Figure 6. Two curves are shown: one averages the errors in a 64-bit window immediately after the preamble, while the other averages such a window in the middle of the burst. In both cases an interfering dummy burst with a separate carrier and clock source was inserted between the bursts under measurement to simulate the TDMA acquisition environment. Note the small discrepancies even at very low error rates.

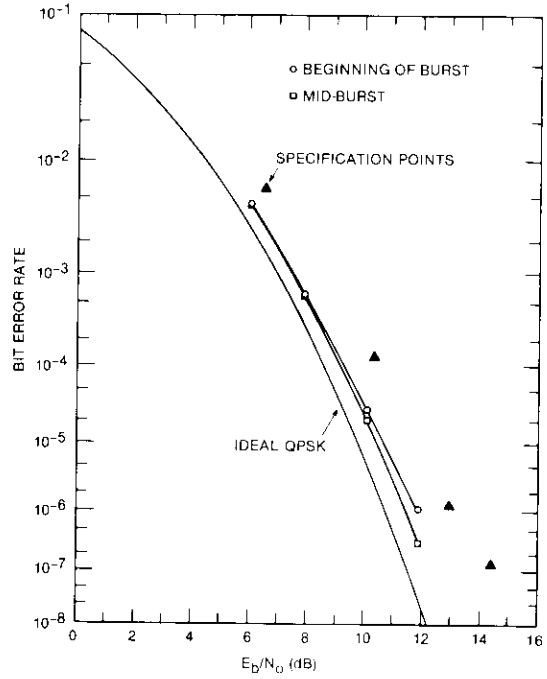


Figure 6. *BER vs E_b/N_0 at Nominal Conditions—Modem 002*

The sensitivity of the feed-forward phase correction technique is illustrated by the BER performance shown in Figure 7. Measurements were made over a range of frequency offsets and amplitude differences between the measurement burst and the dummy burst. These measurements stress the phase

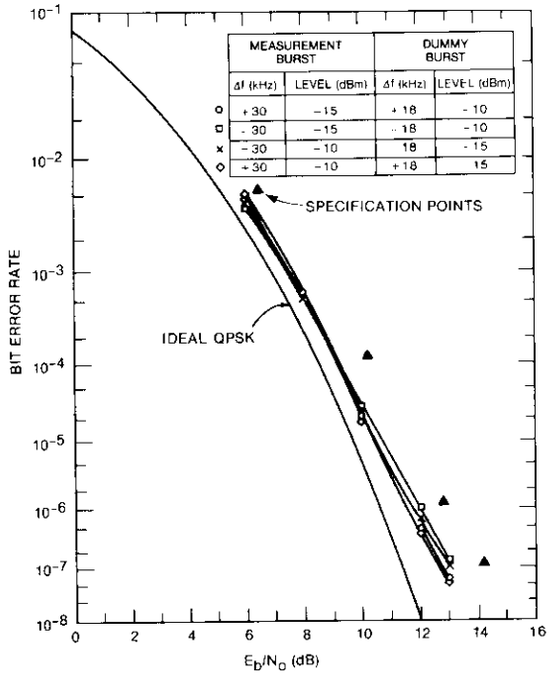


Figure 7. *BER Performance With Amplitude and Frequency Offsets—Modem 002*

correction circuit to its extreme. Little degradation to the BER is observable, even with a dummy burst 5 dB higher than the measured burst.

The most crucial modem design area was achieving the unique word miss probability. The synchronous oscillator is described by Lindsey as governed by a differential equation similar to that of a first order phase-locked loop [12]. The measured probability of unique word miss in Figure 8 shows that the phase-locked loop hang-up phenomenon is not a factor degrading acquisition performance. To illustrate the reproducibility of the results, curves are shown for each of the two modems which were built. Each was tested at zero frequency offset with dummy bursts and for each, a margin greater than 1 dB from the specification was achieved. These measurements were made with a specifically designed burst test set which reproduced the TDMA burst format, including the unique word generator and detector and the dummy burst.

The measured probabilities of carrier and clock cycle slipping are shown in Figures 9 and 10, respectively. Two sets of measurements are again presented for each case. The margin by which the carrier cycle slipping met

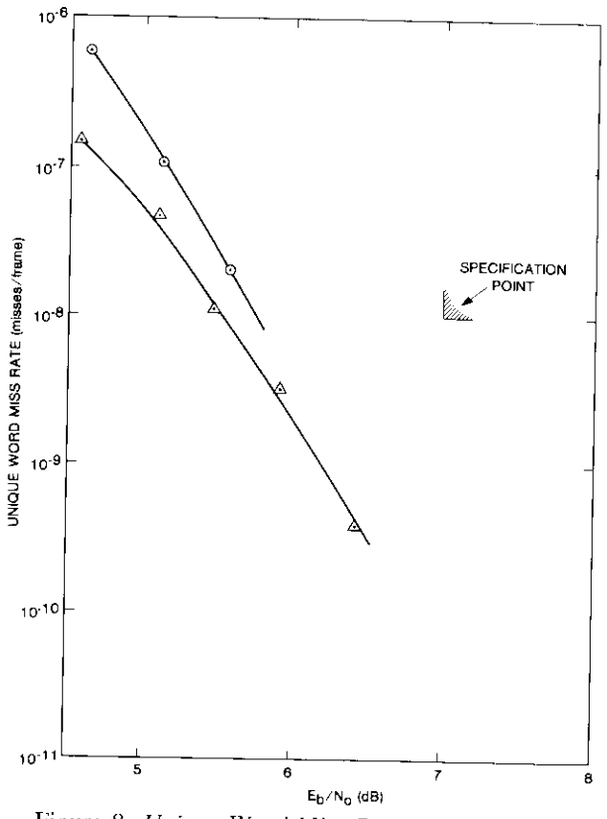


Figure 8. *Unique Word Miss Rate Performance*

the requirements was only 0.4 dB; this is in part due to the difficulty of achieving the relatively narrow bandpass filter bandwidth at the fourth harmonic of the input carrier. This situation could be improved somewhat with better filter implementation or by operation of the carrier recovery at a lower IF frequency. The clock recovery performance shows more than a 2.5-dB margin from the specification and proves the viability of the synchronous oscillator as a clock recovery mechanism for a TDMA modem.

TDMA codec design and performance

The BER objectives of all INTELSAT V TDMA links can be achieved with a rate 7/8 FEC code and a hard-decision decoder of moderate complexity [2]. Where the performance of a hard-decision decoder meets system objectives, block codes have been found superior to convolutional codes for TDMA applications because the block codec does not need initialization and

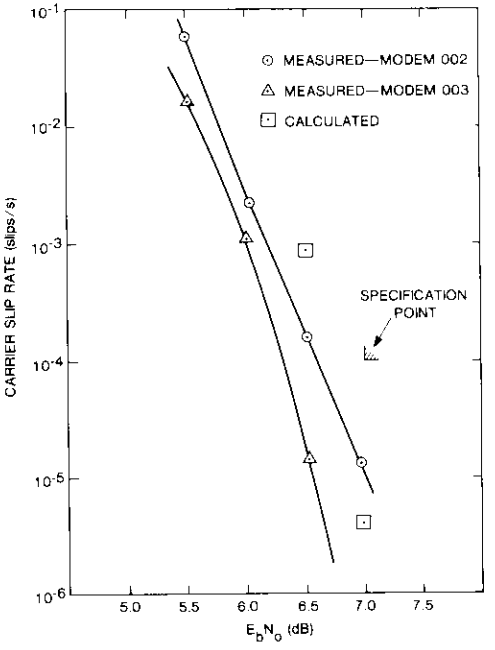


Figure 9. *Carrier Cycle Slip Rate vs E_b/N_o for INTELSAT V Modem*

termination at the beginning and end of each burst, while the convolutional codec does [2], [15].

A unique 8-bit parallel implementation of the INTELSAT-specified (128, 112)* Bose-Chaudhuri-Hocquenghem (BCH) code has been designed as an integral part of the COMSAT Laboratories advanced TDMA terminal. The codec corrects all 1- and 2-bit error combinations within a code block and detects all 3-bit errors. By reducing the codec clock rate to 15 MHz, the parallel structure permits operation at a data rate of 120 Mbit/s with Schottky transistor-transistor logic (TTL) instead of emitter-coupled logic (ECL). In concert with other innovations, the parallel design lowers codec chip count to 127—a reduction of 40 percent over the serial ECL approach.

The following subsections describe the characteristics of the (128, 112) modified BCH code. A description of the codec at the block diagram level is given, followed by discussion of various novel aspects of the 8-bit architecture. Both theoretical error-correction ability and measured hardware results are then presented.

*An (n, k) code is formatted in blocks of n bits, with k the information bits.

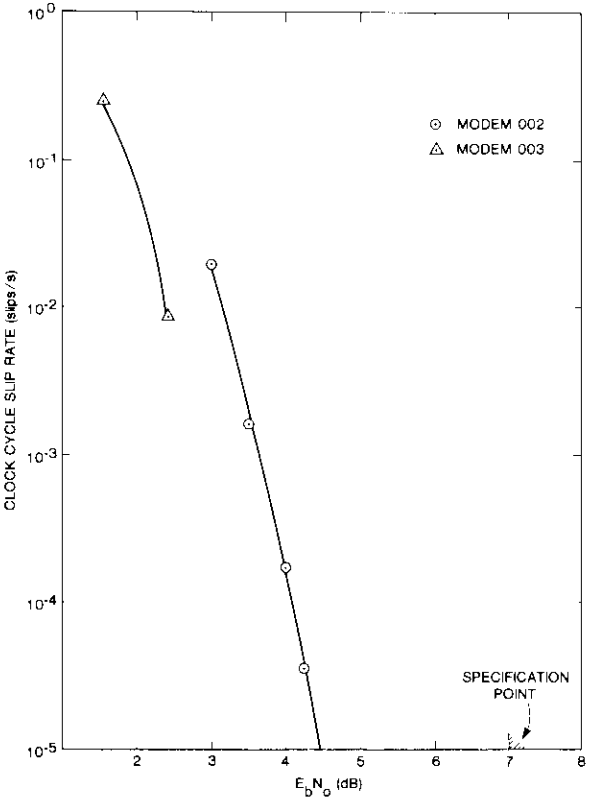


Figure 10. *Clock Slip Rate vs E_b/N_o*

Code characteristics

The (128, 112) modified BCH code has double-error-correcting (DEC) and triple-error-detecting (TED) properties which result from the addition of an overall parity check to a DEC (127, 113) BCH code and the elimination of one information bit. Adding the TED capability avoids false corrections which would occur when three errors are present in one code block that would otherwise result in an average of four output errors. This approach reduces output BER by 25 percent compared to the original DEC code, with only a very small increase in the amount of hardware required.

The generator polynomial of the modified code, $G'(x)$, is obtained by multiplying the original code's polynomial $G(x)$ (see Appendix A) by the term $(x + 1)$, yielding

$$G'(x) = (x + 1)\,G(x)$$
$$= (x + 1)(x^{14} + x^{12} + x^{10} + x^6 + x^5 + x^4 + x^3 + x^2 + 1) \quad (4)$$

or

$$G'(x) = x^{15} + x^{14} + x^{13} + x^{12} + x^{11} + x^{10} + x^7 + x^2 + x + 1 \quad . \quad (5)$$

This multiplication increases the number of check bits per code block from 14 to 15. A dummy bit is added so that the check and information bits are each multiples of eight so as to provide system compatibility, resulting in a (128, 112) BCH code. A complete code block (Figure 11) contains 112 bits of information followed by 15 check bits and a dummy bit. Any polarity is acceptable for the dummy bit, whose only function is filling the parity symbol time slot.

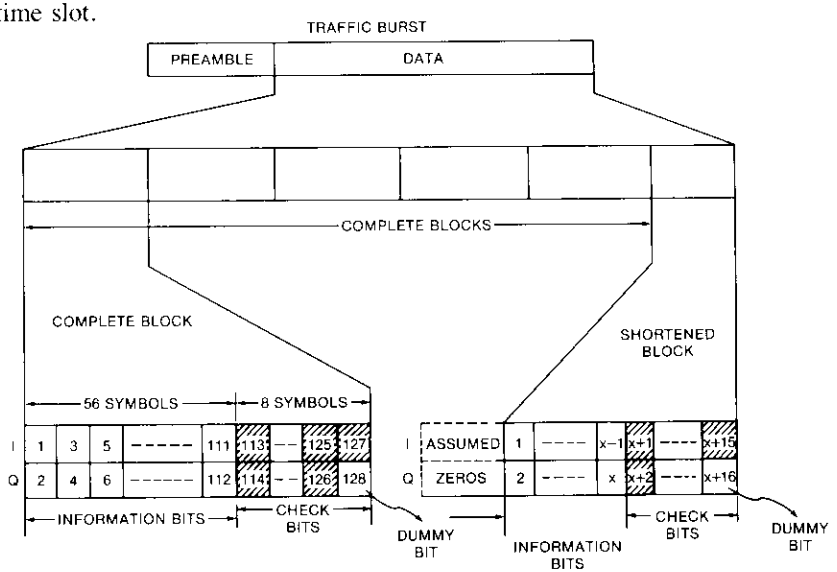


Figure 11. *(128, 112) BCH Code Block Structure*

Since the traffic portion of a TDMA burst is not necessarily an exact multiple of 112 bits, the final code block in a burst will generally contain less than 112 information bits. This shortened block will contain the normal complement of 15 check bits plus one dummy bit. In decoding, zeros are assumed to have preceded the information bits to complete the last block, although the decoder takes no special action regarding these fictitious bits. Instead, short blocks are handled automatically by the codec without any additional padding bits.

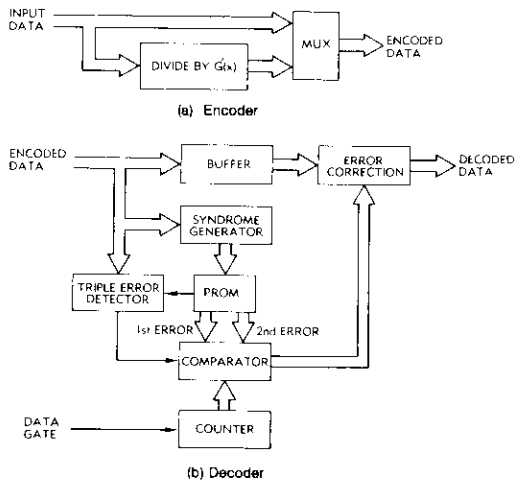


Figure 12. *High-Speed Parallel (128, 112) BCH Codec*

General codec structure

The encoder (Figure 12) divides the block of 112 input bits by the generator polynomial $G'(x)$. The remainder of this calculation forms the check bits which are appended to the end of the data block.

As received data enter a buffer memory in the decoder (Figure 12), the syndrome of the error pattern is simultaneously calculated by dividing the entire received code block by the polynomial $G(x)$. At the end of each 128-bit code block, the syndrome is used to address a location in programmable read-only memory (PROM) that contains the positions of the error bits within the code block. The PROM output consists of two binary numbers representing the locations of up to two errors. These error location numbers are compared to the state of a counter which tracks bit position as data are shifted out of the buffer. When a correctable error appears at the output of the buffer, the comparator produces a correction pulse which is used to invert the erroneous bit.

Comparator function is inhibited when three errors are detected within a code block, thus avoiding false decoder action. Detection of triple errors is accomplished by determining that an odd number of errors greater than one has occurred. Since each code block should contain an even number of 1's, an overall parity check easily determines whether an odd number of errors has occurred. The presence of a single-bit error is readily incorporated into the first error location number since only seven of the eight PROM output bits are needed to specify any bit within a code block. If an odd number of errors

is detected and a 1-bit error is not indicated by the PROM output, the comparator is inhibited to prevent false correction pulses.

Innovative codec design

The codec incorporates several innovative design features, including novel parallel feedback shift register implementations of the encoder and syndrome generator, random-access memory (RAM) data storage, a PROM look-up table, and a novel data counter scheme.

PARALLEL ENCODER IMPLEMENTATION

In a high-speed, bus-oriented TDMA terminal where data occur in 8-bit bytes, a parallel implementation of the encoder is more convenient than the classical serial form (see Appendix B). The parallel encoder accepts a sequence of 112 input bits in the form of 8-bit parallel bytes. After 14 such bytes have been clocked into the parallel feedback shift register, the register contents comprise the desired check bits, which are identical to those produced by a serial encoder.

PARALLEL SYNDROME GENERATION

An 8-bit parallel implementation of the syndrome generator in the decoder is also preferable and may be derived from the more conventional serial configuration in the same manner employed to obtain the parallel form of the encoder (see Appendix B).

The syndrome generator divides the received code block of 112 information bits plus 15 check bits (the dummy bit has no error-correction function) by the polynomial

$$G(x) = \frac{G'(x)}{x + 1} \tag{6}$$

where $G(x)$ is the generator polynomial of the original DEC (127, 113) code which is used in the decoder because the modified (128, 112) code retains the error-correction properties of the original code. The additional check bit contributed by the $(x + 1)$ term provides an overall parity check which permits the detection of triple errors. During syndrome generation, this extra check bit appears as if it were the 113th information bit (which it replaces) in the original code.

A serial syndrome generator would accept 127-bit code blocks while ignoring the dummy bit. However, the parallel syndrome generator processes 128 bits since it accepts sixteen 8-bit bytes. The error-correction capabilities of the code are preserved by treating the 128th bit as a zero during syndrome generation.

The resulting parallel syndrome is identical to that produced by shifting the serial syndrome generator one extra time following the 127th bit. Moreover, this shifted parallel syndrome is the same as the ordinary serial syndrome for an error sequence occurring one bit earlier in the code block. The code block is considered to wrap around on itself so that the parallel syndrome for an error in the first bit is identical to a conventional serial syndrome pattern for an error in the 127th position. The shifted syndrome merely alters the addresses of the stored error location numbers relative to what they would be for a common serial syndrome.

DATA STORAGE AND SYNDROME MAPPING

The decoder contains an RAM buffer which stores the input data to allow time for syndrome generation and look-up table access. Previous designs have used shift registers to accomplish the same objective. The ping-pong RAM input buffer requires only 8 RAM chips and a counter chip to generate control signals, while 32 chips would be required if 8-bit shift registers were used.

Erasable PROMs of 64K (8K × 8) storage capacity are used to form a look-up table which converts each syndrome to a pair of error location numbers. Only four chips are needed to hold the 2^{14} patterns necessary for correction of all single- and double-bit errors.

CONTROL SIGNAL GENERATION

A further improvement involves control signals which must be generated differently in short- and full-block cases. Other designs have used four counters: an input/output pair for full blocks and an additional pair for short blocks. The COMSAT Laboratories codec uses only one data counter to generate the control signals. For full blocks, the counter cycles through its full count. When a short block is identified at the decoder input, the counter output is latched at the end of the short block. The count is then inverted and reloaded into the counter for use in error correction when the short block exits the decoder.

DESIGN ADVANTAGES

A major benefit of the 8-bit parallel structure is that the codec clock rate need only be 15 MHz for a 120-Mbit/s system. This significantly slower clock rate allows the use of Schottky TTL circuits instead of ECL devices. The use of TTL dramatically decreases chip cost and power consumption and also eliminates the need for ECL termination resistors.

This form of 8-bit parallel architecture does not involve repeating a function eight times, but instead involves implementing a single function which

operates on 8-bit parallel data. The parallel feedback shift register contains the same number of register elements as the serial version but employs an exclusive-OR function ahead of each register stage. Parallel-to-serial and serial-to-parallel transformations are eliminated in both the encoder and decoder since the parallel structure is directly compatible with the system data bus. Moreover, the 8-bit data path facilitates use of an efficient RAM data buffer in the decoder, instead of numerous shift registers. The total codec employs only 127 TTL integrated circuits, as compared with 210 ECL chips in a previous design—a reduction in chip count of 40 percent. Thus, the codec requires only a single circuit board and is designed to be an integral part of the TDMA terminal, which simplifies interfacing and minimizes overall system complexity.

Codec performances

The theoretical improvement in error rate is readily predictable for the (128, 112) BCH code and agrees closely with measured performance. A simplified equation is found to provide a convenient approximation of codec error performance.

THEORETICAL ERROR-CORRECTION CAPABILITY

Dividing the complete 127-bit received code block by the polynomial $G(x)$ to produce the syndrome is mathematically equivalent to dividing only the 112-bit received information sequence by $G(x)$ to recalculate the check bits, which are then compared bit-by-bit with the received check bits. With no errors, the original check bits agree with the recalculated bits and the syndrome pattern consists of all zeros. The syndrome pattern is a function only of the error sequence, not of the information sequence [16].

Each 1- and 2-bit error produces a syndrome pattern that points to a unique location in the PROM, permitting all such combinations to be corrected. Moreover, all triple errors in one block are detected, which prevents them from causing additional decoder output errors.

The probability of a decoder output error may be calculated by first noting that the probability of a block of N input bits containing j errors is given by

$$P[j] = \binom{N}{j} p_i^j (1 - p_i)^{N-j} \tag{7}$$

where the errors are assumed to be random, independent, and identically distributed, and the channel bit error probability is p_i [17]. Equation (7) represents the probability of a decoding failure due to exactly j input errors.

The term

$$\binom{N}{j} = N!/[(N - j)!j!]$$

represents the number of combinations of N bits taken j at a time, and the remaining terms give the probability of receiving a particular sequence of j erroneous bits and $(N - j)$ correct bits. Although errors are assumed to be random and independent, no specific distribution is assumed for the channel noise.

The probability of an output bit error may then be expressed [2] by summing the contributions from all input error sequences that exceed the error-correcting capability of the code (*i.e.*, all sequences for which $j \geq t + 1$), to obtain

$$p_o = \sum_{j=t+1}^{N} \frac{e_j}{N} \binom{N}{j} p_i^j (1 - p_i)^{N-j} \tag{8}$$

where e_j = average number of output errors resulting from a code block containing j input errors,
t = number of errors correctable by the code,
N = size of the code block.

A considerably simplified expression for output error probability may be obtained by observing that most decoder output errors are caused by exactly $(t + 1)$ input bit errors and are accounted for by the first term in the summation. Furthermore, the expression $(1 - p_i)^{N-j}$ may be approximated by unity, except at the higher error rates. For the (128, 112) code, t equals 2 and all 3-bit error combinations are detected and produce only three output errors. For full code blocks, the value 127 may be substituted for N to obtain the output bit error probability as

$$p_o \cong 7{,}875\, p_i^3 \tag{9}$$

MEASURED BER REDUCTION

The BER improvement measured in laboratory testing of two units at 120 Mbit/s, shown by the circles and squares of Figure 13, agrees closely with a computed solution of equation (8) for values of $j \leq 5$. The solution

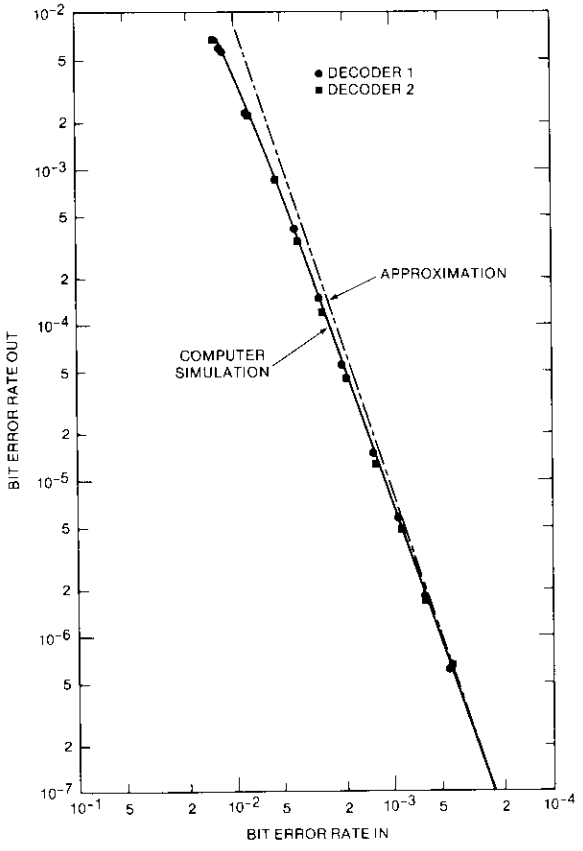


Figure 13. *Error-Rate Reduction of (128, 112) BCH Code*

of equation (8) was obtained as part of a computer simulation of the (128, 112) BCH decoder performance [2], [15]. Equation (9), shown by the dashed line in Figure 13, provides an easy-to-use approximation of error performance which is highly accurate over most of the useful range of the codec.

Operational BER performance

In order to characterize the performance of the 120-Mbit/s QPSK modems in an actual operating environment, two field trials were conducted at the Andover Earth Station using INTELSAT V satellite transponders. The INTELSAT V spacecraft has two transponder bandwidths available for TDMA applications: 72 MHz and 77 MHz. The first field trial was conducted over

a 72-MHz transponder (5–6), while the second used the wider 77-MHz transponder (1–2). The equipment configuration was essentially identical for the two trials and is shown in Figure 14. A special BER test set designed at COMSAT Laboratories was used for error rate measurement.

System equalization and calibration

The transmission system shown in Figure 14 was broken up into three major segments, up-link, satellite transponder, and down-link, with each segment analyzed for its contribution to the overall link distortion and resulting BER degradation. Using commercially available test equipment (a microwave link analyzer), the amplitude and group delay of the up-link and down-link were measured individually. A combination of fixed equalizers and a variable transversal equalizer was then inserted at the modulator output on the up-link and at the demodulator input on the down-link. These equalizers were picked to give flat amplitude and group delay responses. The up-link and down-link responses before and after equalization for the Andover Earth Station are shown in Figures 15 and 16. INTELSAT has specified masks showing maximum permissible amplitude and group delay variations for up- and down-links. They are shown in Figure 17, where it can be seen that the equalized responses fall approximately within these masks.

Because the satellite input multiplex filter has an on-board equalizer, only the output multiplex filter requires equalization in the earth station. Since amplitude and group delay characteristics of this filter are available, an appropriate equalizer was designed and built prior to the actual field trial and inserted in the down-link path. The amplitude and group delay response through the entire system using transponder 5–6 is shown in Figures 18a and 18b, both before and after transponder equalization. The equivalent equalized responses of transponder 1–2 are shown in Figure 18c.

In the operational INTELSAT system, it is anticipated that the station high-power amplifier (HPA) will be operated with at least 10-dB input backoff and the satellite traveling wave tube amplifier (TWTA) at 2-dB input backoff. During the field trials, the HPA drive level was adjusted to operate the satellite at 2-dB input backoff with the HPA operating in a nearly linear mode, that is, at more than 10 dB below the 1-dB compression point.

BER measurements

BER was measured in continuous mode over the equalized links described above. Noise was added on the down-link as shown in Figure 14. The up-link noise contribution was measured, with the satellite TWTA at 2-dB input backoff, by offsetting a continuous wave (CW) carrier to the edge of the transponder frequency band and then measuring noise power with a narrow

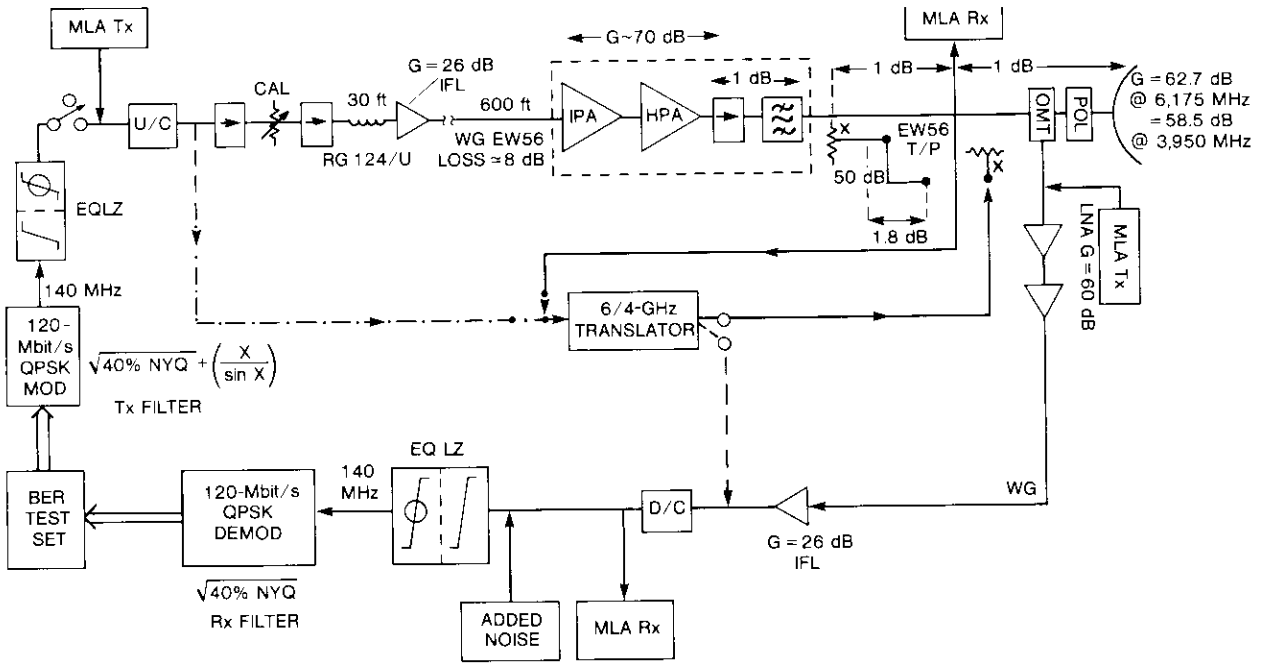
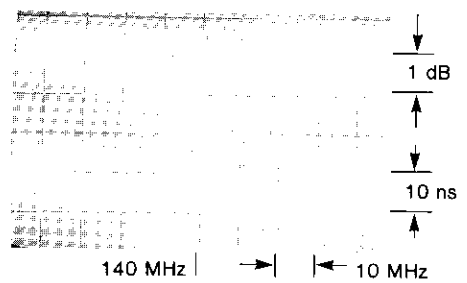
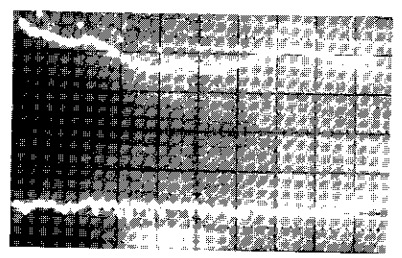


Figure 14. *Simplified Block Diagram of the Measuring Setup*

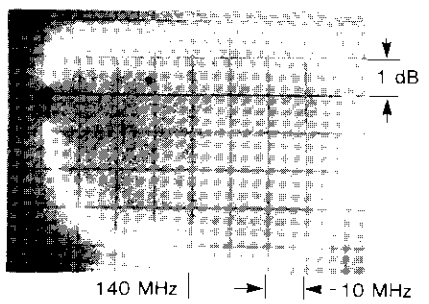


(a) Unequalized Up-Chain Response

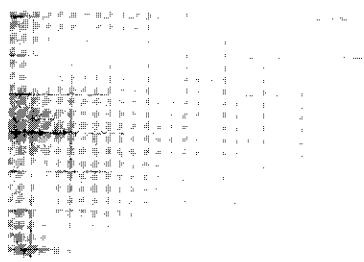


(b) Up-Chain Response Equalized With 5-ns Positive Group Delay Slope and 4-ns Parabolic Group Delay Equalizers

Figure 15. *Earth Station Up-Chain Response*



(a) Unequalized Down-Chain Response



(b) Down-Chain Response Equalized With 9-ns Positive Group Delay Slope and 12-ns Parabolic Group Delay Equalizers

Figure 16. *Earth Station Down-Chain Response*

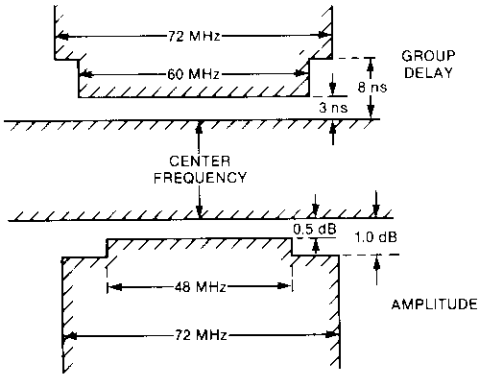


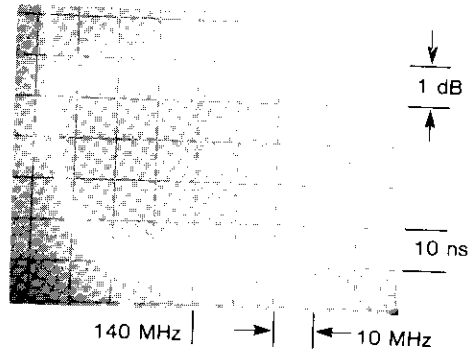
Figure 17. *Group Delay and Amplitude Response Limits*

bandpass filter at the transponder center frequency. The value of the carrier-to-noise (*C/N*) ratio due strictly to the added down-link noise was modified to take into account this constant additive noise.

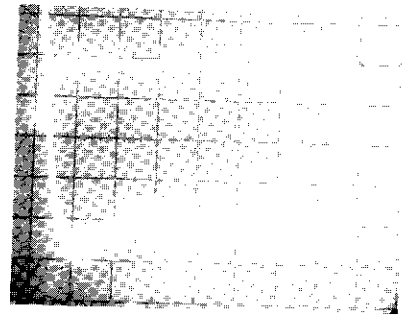
The results for transponder 1–2 and 5–6 are shown in Figures 19 and 20, along with modem IF loopback data. Note that the performance achieved in transponder 5–6 is 1 to 1.5 dB poorer than that achieved in transponder 1–2. Possibly part of this difference is due to the fact that the nominal bandwidth of transponder 5–6 is only 72 MHz, while that of transponder 1–2 is 77 MHz. However, no detailed analysis was done and therefore there may also be other contributing factors, such as differences in up- and down-link characteristics, and differences in TWT characteristics on the spacecraft. Both sets of data are within the specifications set up by INTELSAT for nonlinear channel operation. A slight degradation relative to this performance could be expected if the HPA were operated at 10-dB input backoff.

TDMA transmission system performance

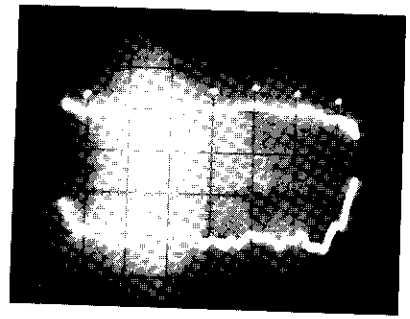
Codec BER performance during TDMA field trial testing over the actual nonlinear INTELSAT V satellite channel (Figure 21) agrees quite well with computer simulation results and may be directly compared with the laboratory measurements (Figure 13) of the codecs alone. The simulation performance is based on the assumption of random, independent errors and is not directly related to channel linearity. However, intersymbol dependencies arising from channel filtering and timing recovery circuits will cause deviation from the simulated results. The results of Figure 21 indicate that such dependencies were minimal for the test channel and that differences between theory and practice can be largely attributed to experimental variations.



(a) Unequalized Transponder (5-6)



(b) Equalized Transponder (5-6)



(c) Equalized Transponder (1-2)

Figure 18. *System Frequency Response*

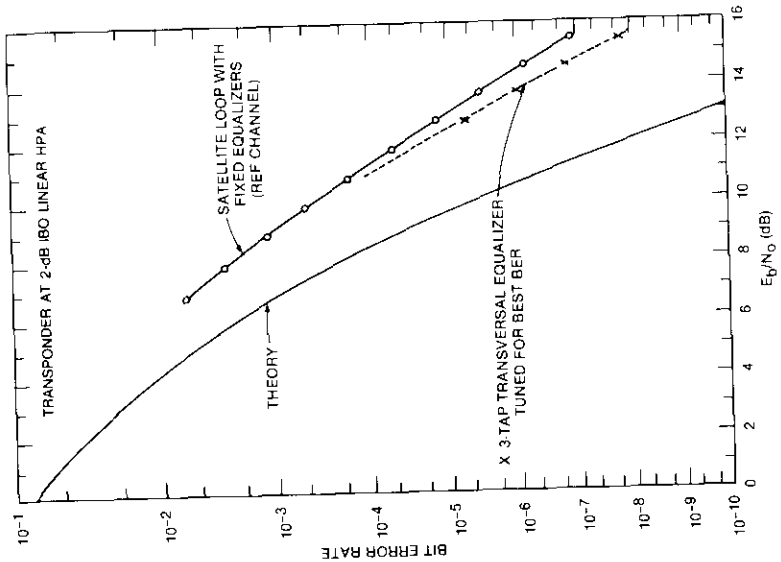


Figure 20. *Link BER Performance: Transponder 5–6*

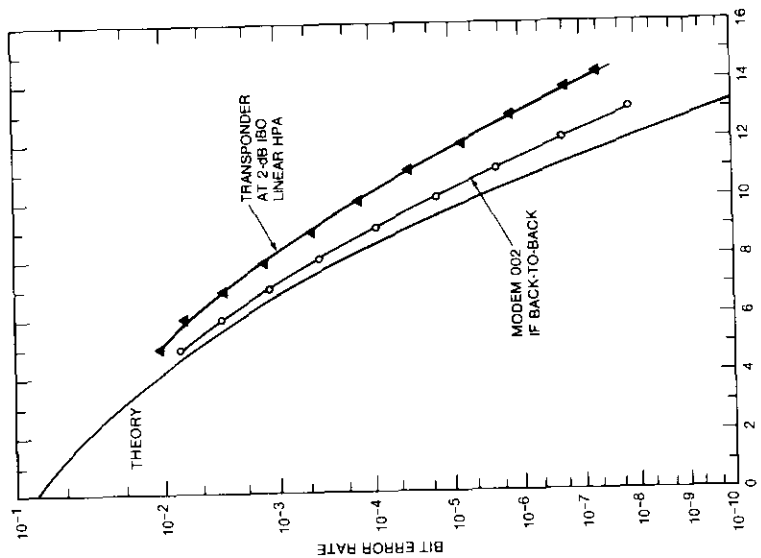


Figure 19. *Link BER Performance (BER vs E_b/N_0): Transponder 1–2*

Link sensitivity measurements

After the channel 5–6 link was equalized for flat response and its performance measured, known values of amplitude and group delay distortion were added in both the up- and down-link. The BER performance with linear amplitude slope is shown in Figure 22. Figures 23 and 24 demonstrate the effects of added linear and parabolic group delay distortion. In some cases, the added distortion is partially compensating for network elements such as modem filters and amplifiers, as well as transmission path amplifiers and bandpass filters which have not been ideally equalized. This results in unequal degradation from distortions of equal magnitude and type, but of opposite polarity.

Conclusions

The research which has been conducted on the development of modems and FEC codecs for application to the INTELSAT V satellite system has resulted in a modem and codec design that has achieved all of the goals set down during the development of the system specification. The measurements of BER for both linear and nonlinear channels verify the choice of transmit and receive filters. The acquisition, unique word miss performance, and the cycle skipping measurements have shown that the use of a feed-forward frequency multiplication carrier recovery approach, together with the simplicity of a synchronous oscillator clock recovery circuit, can achieve excellent acquisition performance while maintaining robust performance at low *S/N* ratio. Moreover, the achievable cycle skipping performance was well within the desired goals. The modem performance was also very robust with respect to the degradations introduced by burst-to-burst level and frequency variations and maintained good performance with link perturbations. The FEC codec performed equally well in both the linear and nonlinear channel environments and was easily integrated into the TDMA terminal. Finally, two separate field tests have demonstrated that the performance required for the INTELSAT TDMA system can be achieved in an operational environment.

Acknowledgments

The authors wish to acknowledge the significant contributions of W. Hersey for the detailed design and testing of the codec, and D. Chakraborty for the field measurements of modem performance.

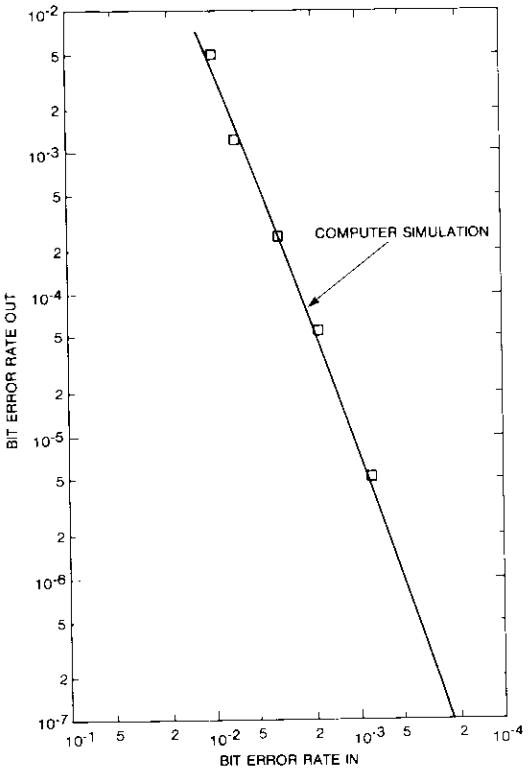


Figure 21. *Error Rate Reduction of (128, 112) BCH Code Over Nonlinear Satellite Channel*

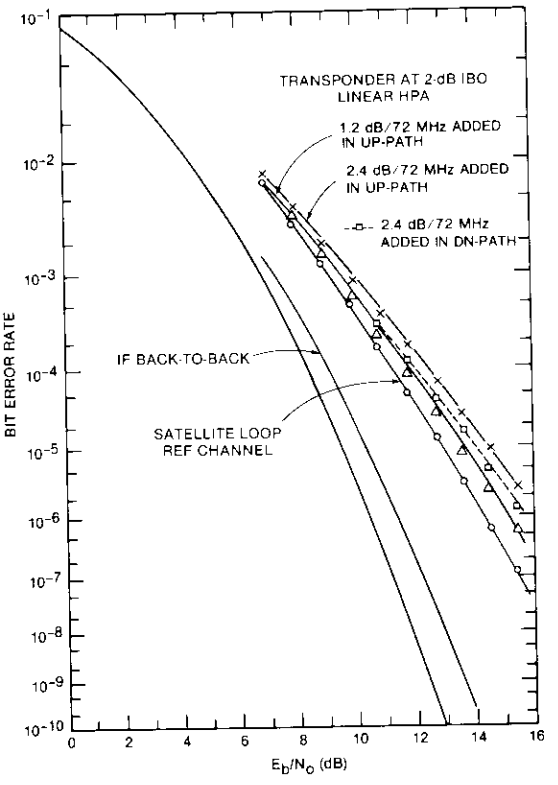


Figure 22. *Channel Sensitivity Due to Amplitude Distortion*

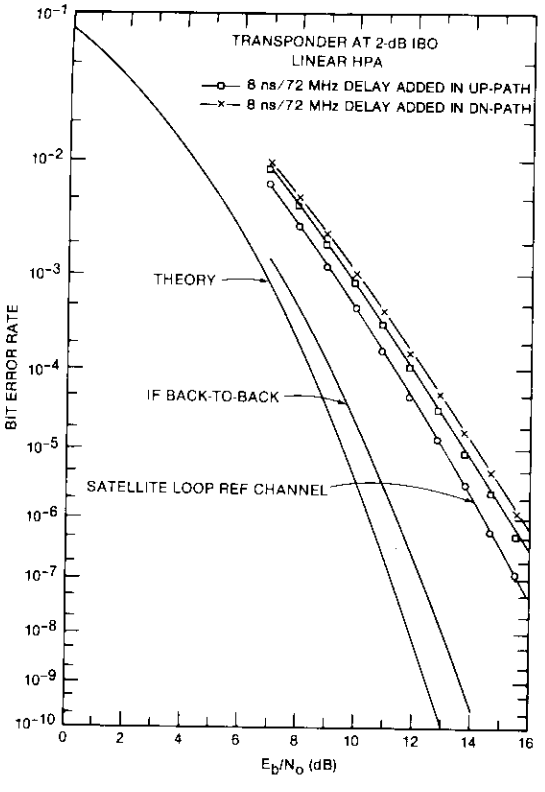


Figure 23. *Channel Sensitivity Due to Linear Delay Distortion*

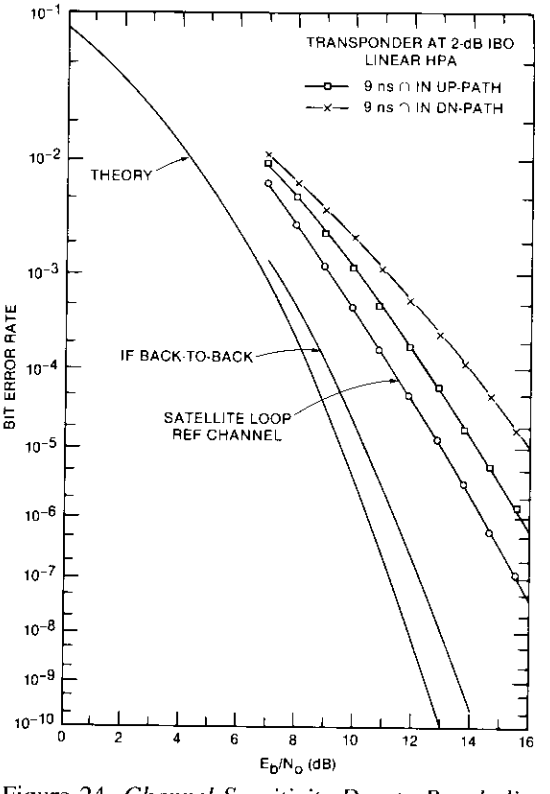


Figure 24. *Channel Sensitivity Due to Parabolic Delay Distortion*

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Appendix A. Derivation of (128, 112) BCH code generator polynomial

The generator polynomial, $G'(x)$, of both the DEC/TED (127, 112) BCH code and the (128, 112) code formed by adding a dummy bit is obtained by multiplying the generator polynomial, $G(x)$, of the DEC (127, 113) BCH code by the factor $(x + 1)$ to obtain

$$G'(x) = (x + 1)\, G(x) \quad . \tag{A-1}$$

The generator polynomial of the parent code, $G(x)$, is the least common multiple of the odd minimum polynomials m_i for $i = 1, 3, \ldots, 2t_0 - 1$ [16] or

$$G(x) = \text{LCM}\,[m_1(x), m_3(x), \ldots, m_{2t_0 - 1}(x)] \tag{A-2}$$

where t_0 is the designed error-correcting capability of the code.

The minimum polynomial $m_i(x)$, also known as the minimum function of α^i, is given by the product

$$\begin{aligned} m_i(x) = {} & [x + \alpha^i][x + \alpha^{2i}][x + \alpha^{4i}][x + \alpha^{8i}] \ldots \\ & \cdot [x + \alpha^{(2^m - 1)i}] \end{aligned} \tag{A-3}$$

where α is a primitive element of the Galois field of 2^m elements, $GF(2^m)$.

For the (127, 113) code, t_0 equals 2. Therefore, from equation (A-2), its generator polynomial may be expressed as

$$G(x) = \text{LCM}\,[m_1(x), m_3(x)] \quad .$$

The minimum polynomial $m_1(x)$ may be chosen to be the primitive polynomial

$$m_1(x) = x^7 + x + 1 \quad .$$

The problem then reduces to computing $m_3(x)$, given that $m_1(\alpha) = 0$, *i.e.*,

$$\alpha^7 = \alpha + 1 \quad .$$

Moreover, $m = 7$ for the (127, 113) code and, since α is a primitive element of $GF(2^7)$,

$$\alpha^{127} = 1 \quad .$$

The polynomial $m_3(x)$ may be easily written according to equation (A-3) by first writing the corresponding sequence of ascending powers of α^i until the sequence repeats. For $i = 3$, this process yields

$$\alpha^3, \alpha^6, \alpha^{12}, \alpha^{24}, \alpha^{48}, \alpha^{96}, \alpha^{192} = \alpha^{127} = \alpha^{65}, \alpha^{130} = \alpha^{127}\alpha^3 = \alpha^3.$$

Therefore, the desired minimum polynomial is given by

$$m^3(x) = (x + \alpha^3)(x + \alpha^6)(x + \alpha^{12})(x + \alpha^{24})(x + \alpha^{48}) \cdot (x + \alpha^{65})(x + \alpha^{96}) \quad . \tag{A-4}$$

To expand $m_3(x)$ and evaluate the coefficients of the various powers of x, it is helpful to make use of a partial listing of the 2^7 elements of $GF(2^7)$ formed as the field of polynomials over $GF(2)$ modulo $x^7 + x + 1$. Such a listing is given in Table A-1. After a considerable amount of algebraic manipulation, it may be shown that equation (A-4) reduces to

$$m_3(x) = x^7 + x^5 + x^3 + x + 1 \quad .$$

Therefore,

$$G(x) = \text{LCM}\,[m_1(x), m_3(x)] = (x^7 + x + 1)(x^7 + x^5 + x^3 + x + 1)$$

or

$$G(x) = x^{14} + x^{12} + x^{10} + x^6 + x^5 + x^4 + x^3 + x^2 + 1 \quad .$$

From equation (A-1),

$$G'(x) = (x + 1)\,G(x)$$

or

$$G'(x) = x^{15} + x^{14} + x^{13} + x^{12} + x^{11} + x^{10} + x^7 + x^2 + x + 1 \quad .$$

TABLE A-1. ELEMENTS OF $GF(2^7)$ WHERE α IS A ROOT OF $x^7 + x + 1$

0
$\alpha^0 = 1$
$\alpha^1 = \alpha$
α^2
α^3
α^4
α^5
α^6
$\alpha^7 = \alpha + 1$
$\alpha^8 = \alpha\alpha^7 = \alpha^2 + \alpha$
$\alpha^9 = \alpha\alpha^8 = \alpha^3 + \alpha^2$
$\alpha^{10} = \alpha\alpha^9 = \alpha^4 + \alpha^3$
$\alpha^{11} = \alpha\alpha^{10} = \alpha^5 + \alpha^4$
$\alpha^{12} = \alpha\alpha^{11} = \alpha^6 + \alpha^5$
.
.
.
$\alpha^{24} = \alpha^{12}\alpha^{12} = \alpha^6 + \alpha^5 + \alpha^4 + \alpha^3$
.
.
.
$\alpha^{48} = \alpha^5 + \alpha^4 + \alpha^3 + \alpha^2 + \alpha$
.
.
.
$\alpha^{65} = \alpha^5 + \alpha^2$
.
.
.
$\alpha^{96} = \alpha^6 + \alpha^3 + \alpha$
.
.
.
$\alpha^{126} = \alpha^6 + 1$

Appendix B. Parallel codec derivation

This appendix describes the method for deriving the parallel feedback shift register structures for the encoder and syndrome generator from their conventional serial forms.

Parallel encoder derivation

A classical serial encoder divides the input sequence by the generator polynomial $G'(x)$ using a feedback shift register (Figure B-1). The remainder which results from this division constitutes the check bits. Each input bit is added modulo 2 (*i.e.*, exclusive-ORed) with the contents of the last stage of the register to form the feedback signal. Connecting the input to the last stage in this manner is equivalent to premultiplying the input sequence by x^{15} before dividing by the generator polynomial [16]. The result of this premultiplication is that the register contains the 15-bit remainder as soon as the last of the 112 information bits in each block is entered, avoiding the need for additional shifting to complete the division process. The remainder is shifted out of the register to form the 15 check bits which immediately follow the 112 information bits in each code block.

Converting the serial encoder to parallel form may be accomplished by first writing a family of equations expressing the contents of each stage of the serial register after the next shift, in terms of the current contents and the current input bit. From these, a similar set of equations may be written expressing the contents of each stage after eight such shifts. Finally, this new set of equations may be solved to express the contents of each stage after eight shifts, in terms of the present contents and eight consecutive input bits. The resulting equations describe an 8-bit parallel equivalent of the serial encoder.

The equations may also be derived through matrix operations by first expressing the contents of the serial register after the next shift as

$$\begin{aligned} p_{15}(t+1) &= p_{14}(t) + p_{15}(t) + i(t) \\ p_{14}(t+1) &= p_{13}(t) + p_{15}(t) + i(t) \\ &\vdots \\ p_1(t+1) &= p_{15}(t) + i(t) \end{aligned} \qquad \text{(B-1)}$$

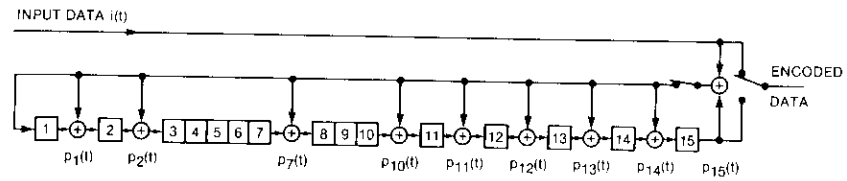
where the $p_i(t)$ are the contents of each stage of the register at time t, $i(t)$ is the input bit at time t, and addition is modulo 2.

In matrix form,

$$|p(t+1)| = [T]\,|p(t)| + |G|\,i(t) \qquad \text{(B-2)}$$

where

$$|p(t)| = \begin{bmatrix} p_{15}(t) \\ p_{14}(t) \\ \vdots \\ p_1(t) \end{bmatrix}$$



$$G'(x) = (x+1)(x^{14} + x^{12} + x^{10} + x^6 + x^5 + x^4 + x^3 + x^2 + 1)$$
$$= x^{15} + x^{14} + x^{13} + x^{12} + x^{11} + x^{10} + x^7 + x^2 + x + 1$$

Figure B-1. *Serial (128, 112) BCH Encoder*

The 15 × 15 matrix $[T]$ consists of the coefficients of the $p_i(t)$ in equation (B-1) and represents the serial feedback connections. The column matrix $[G]$, whose elements are the coefficients of the generator polynomial, describes the input connections.

It may be shown that the matrix $[T]^8$ completely describes the equivalent parallel encoder with an 8-bit input bus. Moreover, $[T]^8$ need not be calculated explicitly because its elements may be rapidly hand-calculated by a procedure based upon eight shifts of the serial register with a single binary-1 input [18].

Regardless of the technique used, the final family of equations is

$$\begin{aligned} p_{15}(t+8) &= p_7(t) + p_8(t) + p_{13}(t) + p_{14}(t) + p_{15}(t) \\ &\quad + i(t) + i(t+1) + i(t+2) + i(t+7) \\ p_{14}(t+8) &= p_6(t) + p_8(t) + p_{12}(t) + p_{15}(t) \\ &\quad + i(t) + i(t+3) + i(t+7) \\ &\vdots \\ p_1(t+8) &= p_8(t) + p_9(t) + p_{14}(t) + p_{15}(t) + i(t) \\ &\quad + i(t+1) + i(t+6) + i(t+7) \quad . \end{aligned} \qquad \text{(B-3)}$$

Equation (B-3) describes a parallel structure (Figure B-2) in which $i(t)$, $i(t+1)$, . . . , $i(t+7)$ represent the current 8 bits on a parallel input bus, the $p_i(t)$ represent the current register contents, and the $p_i(t+8)$ represent the contents of the register after the next shift.

The resulting parallel BCH encoder accepts a sequence of 112 input bits in the form of 8-bit parallel bytes. After the last byte is clocked into the parallel encoder, the register contents $|p_{15}(t), p_{14}(t), \ldots, p_1(t)|$ comprise the desired check bits.

Parallel syndrome generator

The syndrome generator may be implemented in the standard serial fashion (Figure B-3), which is similar to the serial encoder. One less shift-register stage is required for the syndrome generator than for the encoder because the degree of $G(x)$

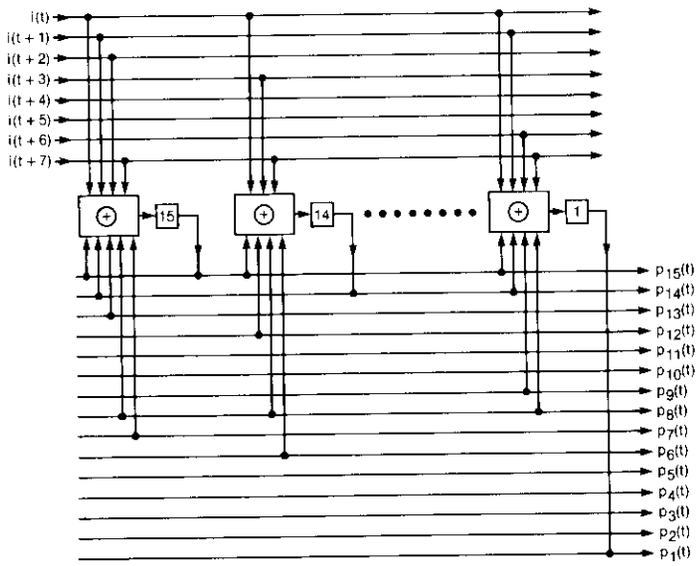
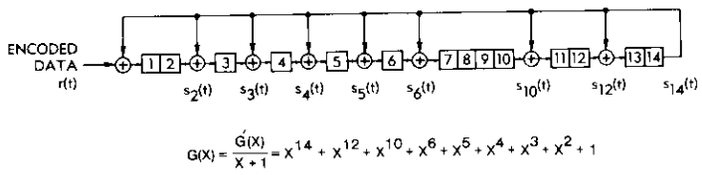


Figure B-2. *Parallel (128, 112) BCH Encoder*



$$G(X) = \frac{G'(X)}{X+1} = X^{14} + X^{12} + X^{10} + X^6 + X^5 + X^4 + X^3 + X^2 + 1$$

Figure B-3. *Serial (128, 112) BCH Syndrome Generator*

is one less than that of $G'(x)$. Furthermore, the received message is introduced only into the first stage, since premultiplication is not desired in this case.

A byte-parallel implementation of the syndrome generator is more desirable for high-speed TDMA and may be derived from the serial configuration in the same manner employed to obtain the parallel form of the encoder. A family of equations expressing the state of the serial syndrome register at time $(t + 1)$ in terms of the state at time t and the received message bit at time t may be written by inspection of Figure B-3 as

$$\begin{aligned} s_{14}(t+1) &= s_{13}(t) \\ s_{13}(t+1) &= s_{12}(t) + s_{14}(t) \\ &\vdots \\ s_1(t+1) &= r(t) + s_{14}(t) \end{aligned} \tag{B-4}$$

where the $s_i(t)$ are the contents of each stage of the shift register at time t, $r(t)$ is the received message bit at time t, and addition is modulo 2.

As in the case of the encoder, either matrix operations or direct manipulation of the individual equations may be employed to express the state of the syndrome register at time $(t + 8)$ in terms of its state at time t and eight consecutive received bits as

$$\begin{aligned} s_{14}(t+8) &= s_6(t) + s_8(t) + s_{12}(t) \\ s_{13}(t+8) &= s_5(t) + s_7(t) + s_{11}(t) + s_{14}(t) \\ &\vdots \\ s_1(t+8) &= s_7(t) + s_9(t) + s_{13}(t) + r(t+7) \quad . \end{aligned} \tag{B-5}$$

Equation (B-5) describes a parallel syndrome generator structure (Figure B-4) in which $r(t)$, $r(t + 1)$, . . . , $r(t + 7)$ represent the current eight received bits on a parallel bus, $s_i(t)$ represents the current syndrome register contents, and $s_i(t + 8)$ represents the register contents after the next shift.

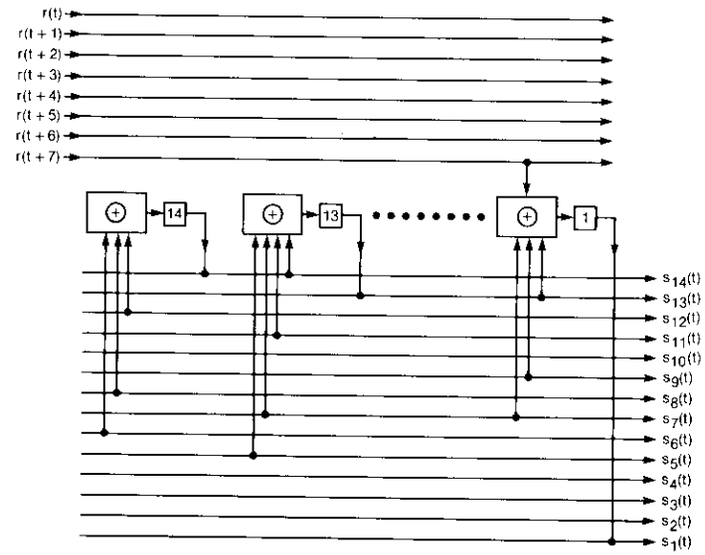


Figure B-4. *Parallel (128, 112) BCH Syndrome Generator*

Chester J. Wolejsza, Jr., received a B.S.E.E. from Cooper Union in 1965, an M.S.E.E. from the Massachusetts Institute of Technology in 1967, and a Ph.D. in Electrical Engineering from the Catholic University of America in 1980. He joined COMSAT Laboratories in 1967, where he developed modems for SPADE, TDMA, and MARISAT applications. In 1975, he became Manager of the Modulation Techniques Department of the Communications Technology Division, with responsibility for supervising the design and development of PSK modulation and coding systems which perform optimally in the band- and power-limited environment of a satellite communications channel. This included work on single-channel-per-carrier techniques, advanced TDMA modulation systems, and specialized modulation and coding equipment for small terminals. In 1985, he joined the Network Products Division of COMSAT Technology Products as Manager of the Modem Engineering Department, where his responsibilities include the design, development, and integration of modulation and coding equipment for the STARCOM product line, which provides VSAT data networks for distributed data processing and computer communications. Dr. Wolejsza has authored papers on modulation systems for professional journals and numerous international conferences. He has been a member of Tau Beta Pi and Eta Kappa Nu, and an associate of Sigma Xi. He is currently a Senior Member of IEEE.

John S. Snyder received a B.S.E.E. from Rochester Institute of Technology in 1965 and an M.S.E.E. from the University of Rochester in 1973. He joined COMSAT Laboratories in 1973 and is presently a Staff Scientist in the Image Processing and Digital Techniques Department, where he is engaged in the research and development of error-correction coding and other digital signal processing techniques applied to satellite communications. Previously, with Taylor Instrument Company and the Department of Defense, he was involved in research and development in the areas of analog and digital signal processing and CRT display systems. Mr. Snyder is a member of the IEEE and holds a number of patents in the areas of error-correction coding and signal processing. He has written several technical papers for international satellite communications conferences, and has authored a variety of papers appearing in technical publications.

Mark Kappes received a B.S.E.E. and an M.S.E.E. from the University of Illinois in 1971. Since joining COMSAT Laboratories in 1979, he has been involved with the design of high-bit-rate modems and satellite link equalization equipment. As Manager of the Transmission Processing Department, he is responsibile for ongoing work in satellite modem technology and associated transmission link equipment. Previously, Mr. Kappes was employed by the Watkins-Johnson Company, where he was responsible for the design of low-noise, high-dynamic-range receivers and special purpose demodulators.

Index: TDMA, transmit timing, receive timing, acquisition, synchronization, satellite position determination

TDMA terminal acquisition and synchronization

G. Forcina and R. Bedford

(Manuscript received June 24, 1985)

Abstract

This paper describes the key timing features of the INTELSAT 120-Mbit/s time-division multiple-access (TDMA) system. The interaction of the reference and traffic terminals is illustrated, and the structure of the communications channels carrying the control information is discussed. The subjects of terminal receive and transmit timing and the associated acquisition and synchronization procedures are specifically addressed, and results and conclusions derived from testing and implementation activities are summarized.

Introduction

The time-division multiple-access (TDMA) technique is based on synchronized, sequential time sharing of transponder resources by the terminals participating in the network. Extensive studies of this key TDMA feature were performed during the early stages of the INTELSAT 120-Mbit/s TDMA system design. These studies resulted in selection of the baseline approach for acquisition and synchronization in the TDMA network. This approach was implemented by selecting the appropriate network architecture and identifying the proper requirements for the reference and traffic terminals during the specification development phase. This paper describes the key elements of the acquisition and synchronization system and their implementation in the selected network architecture.

Network architecture

The general design of the INTELSAT TDMA/digital speech interpolation (DSI) system has been described by Pontano *et al.* [1],[2]. This paper discusses only the elements of the network architecture that pertain to the acquisition and synchronization functions.

In the INTELSAT V TDMA system, the predominant type of connectivity is East-to-West and West-to-East. Since the presence of loopback links cannot be guaranteed, a form of cooperative synchronization control is necessary. The function of feeding back burst position information to the originating terminal is assigned to dedicated network control stations, referred to as reference stations, which provide timing and synchronization control to the TDMA terminals in the network. In order to perform these functions, the reference stations must monitor all TDMA transponders. Thus, it is necessary to employ a minimum of two reference stations, one in the West Zone (and West Hemi) beam and one in the East Zone (and East Hemi) beam. The network configuration is actually based on the use of two reference stations per zone, both simultaneously active, to meet system reliability requirements. Of these two stations, the one which has the primary role is obeyed by its controlled terminals. The other, which is designated as Secondary, is obeyed only during temporary failures of the Primary. In case of prolonged failure of the Primary, the Secondary will assume the Primary role. Figure 1 shows this system configuration for an East-to-West and West-to-East connectivity.

A 2-ms frame and a 16-frame multiframe have been established for the system. The unique words of the reference bursts and traffic bursts change every 16 frames to mark the beginning of the multiframe. These special unique words are referred to as multiframe markers. An important requirement of the synchronization system is that all multiframe markers appear in the same frame at the satellite. This alignment of the multiframe markers at the satellite defines a common multiframe for the system which permits burst time plan rearrangements without loss of traffic.

System control and management information is transmitted by the reference stations to their controlled terminals via the control and delay channel (CDC) and the service channel (SC). The reference burst format, showing the CDC and the SC, is depicted in Figure 2. A message in either the SC or the CDC consists of a 32-bit word transmitted over one multiframe at the rate of 2 bits per frame. For redundancy, each bit is repeated eight times so that 16 bits or 8 symbols are required in each burst for either the CDC or the SC. Figure 3 shows the CDC and SC message format for the P and Q channels of the QPSK modulation scheme employed.

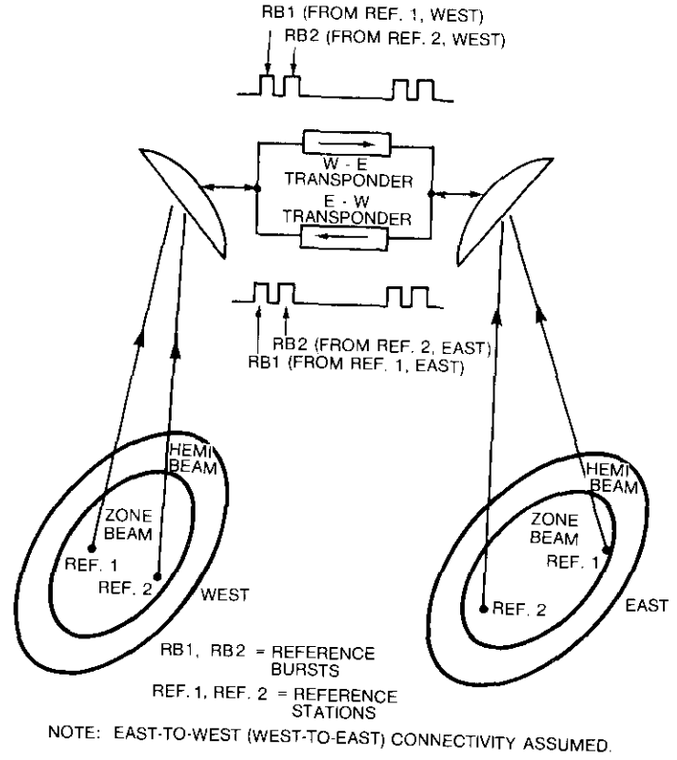


Figure 1. *TDMA System Configuration*

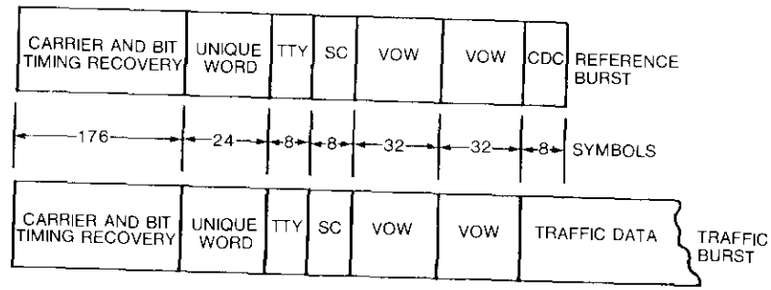


Figure 2. *Burst Format*

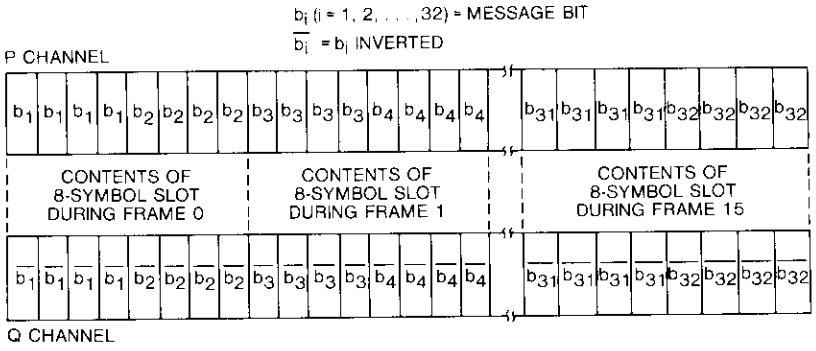


Figure 3. *Format of Message Transmitted via the SC or CDC*

Acquisition and synchronization information is transmitted from the reference stations to the controlled TDMA terminals in the CDC. Thirty-two terminals are addressed cyclically, each with a 32-bit message transmitted over one multiframe. Only 28 of the 32 terminal addresses correspond to actual traffic terminals; the remaining 4 are used for either reference terminals or housekeeping functions. The same terminal is addressed once every 32 multiframes, or 1,024 ms. This 32-multiframe information distribution cycle is referred to as the control frame. The reference bursts transmitted by a reference station into different satellite transponders may contain either the same CDC or different CDCs for a maximum of two CDCs. The control frames of each of the two reference bursts in a transponder are synchronized and contain identical information. Therefore, one pair of reference stations can provide acquisition and synchronization support for up to 56 traffic terminals. Up to 112 traffic terminals can be supported by the four reference stations of a TDMA network.

The SC messages are generated on an as-needed basis and are transmitted according to a priority table. The reference burst SC carries network management messages such as malfunction detection codes and coordination messages for burst time plan changes. The traffic burst SC carries acknowledgment messages and alarm codes.

Network timing

Receive timing is established at the TDMA terminals by detecting the reference bursts. Transmit timing is generally derived from the receive timing by adding the transmission delay provided by the controlling reference station(s). However, the Master Primary reference station obtains its transmit timing from a local high-stability (cesium-beam) clock and constitutes the basic source of timing for the entire network. A long-term timing accuracy of 10^{-11} is achieved which permits the use of a plesiochronous interface for interconnection with national digital networks.

If connectivity is only East-to-West (and West-to-East), the Master Primary station provides a constant transmission delay to the Primary, since the Master Primary cannot perform frame position measurements of the Primary reference burst. In this case, the Master Primary and Primary bursts are not synchronized at the satellite. However, this is of no consequence since no TDMA station can receive both East down-beam transponders and West down-beam transponders.

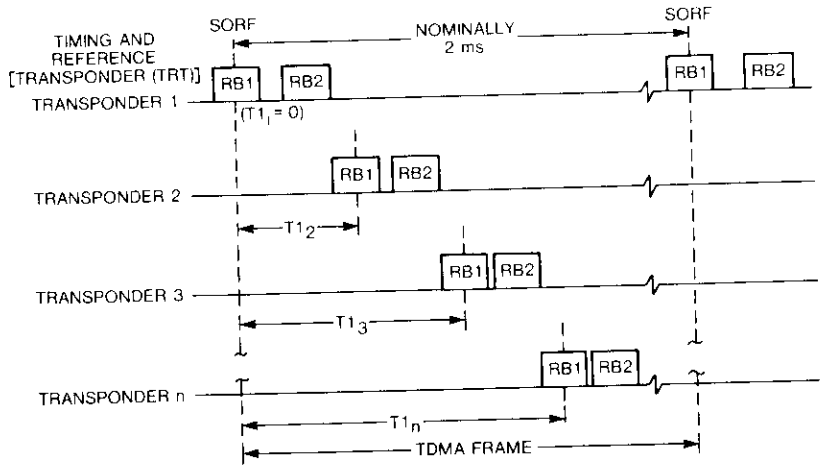
When a beam is connected in a loopback configuration in addition to an East-to-West (West-to-East) connectivity, all transponders must be synchronized because a single TDMA terminal may receive both a loopback transponder and a transponder containing bursts transmitted from the opposite coverage area. In this case, the Master Primary reference burst and the Primary burst must be synchronized. This can be achieved easily, since the Master Primary station can perform frame position measurements of the Primary burst using its own loopback Primary burst as frame reference.

Control of Secondary reference stations is based on burst position measurements, regardless of the form of connectivity. In this respect, Secondary reference stations behave like traffic terminals.

Terminal receive timing

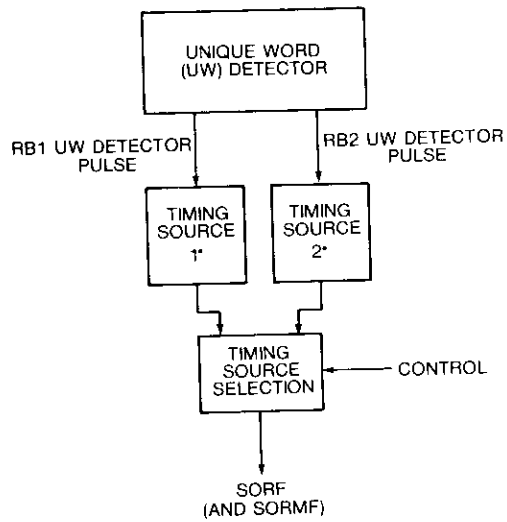
A TDMA terminal derives receive frame timing from the reference bursts received from the TDMA transponders. Figure 4 shows the time relationship between these bursts. The two reference bursts, RB1 and RB2, originate from the two reference stations in a zone coverage area. The start-of-receive frame (SORF) is defined by the time of occurrence of RB1 in the timing and reference transponder (TRT). The SORF can also be derived indirectly by decoding any other reference burst in any transponder, since the time offset from RB1 in the TRT is preassigned for each burst.

The receive side of a TDMA station contains two functional blocks which are referred to as timing sources 1 and 2. Each is phase locked to the unique word detection pulses derived from reference bursts RB1 and RB2, respectively, as shown in Figure 5. Both timing sources have a 512-frame flywheel capability. The terminal SORF is derived from either time source 1 or time source 2, in accordance with the simplified selection table presented in Table 1. The selected timing source provides not only the SORF, but also the start-of-receive multiframe (SORMF), since the reference burst unique word also serves as a multiframe marker.



NOTE: TRAFFIC BURSTS MAY APPEAR BETWEEN RB1 AND RB2 AND BEFORE RB1.

Figure 4. *Time Relationship Between Reference Bursts in Different Transponders*



* REFERENCE BURST OFFSET FROM RB1 IN TRT KNOWN.

Figure 5. *Derivation of Receive Timing*

TABLE 1. SIMPLIFIED DECISION TABLE FOR TIMING SOURCE SELECTION*

			RB1			
			Missed for Less Than 512 Frames			Missed for More Than 512 Frames
			P	S	I	
RB2	Missed for Less Than 512 Frames	P	X	TS2	TS2	TS2
		S	TS1	X	TS2	TS2
		I	TS1	TS1	X	TL
	Missed for More Than 512 Frames		TS1	TS1	TL	TL

*where P = Primary or Master Primary reference burst
S = Secondary reference burst
I = Inoperative reference burst. (A reference burst displays the inoperative status code when re-entering the TDMA frame.)
TS1 = Timing source 1 selected
TS2 = Timing source 2 selected
TL = Timing lost
X = This condition cannot occur

Terminal transmit timing

In all traffic and reference terminals (except the Master Primary), the start-of-transmit frame (SOTF) is obtained from the SORMF. The start-of-transmit multiframe (SOTMF) is generated by applying a transmission delay, D_n, to the SORMF. The SOTF is obtained by dividing the SOTMF into 16 equal intervals, using a local clock.

The SOTF is established via a two-phase process. In the first (acquisition) phase, an acquisition delay is provided by the controlling reference station such that an initial SOTF is obtained which is offset from the final SOTF. The TDMA station uses this initial SOTF to transmit a short burst (preamble only), in accordance with the burst time plan. The initial SOTF is such that the short burst falls within a temporary acquisition window allocated in the frame to accommodate initial position uncertainty. The transmission delay is then changed by the controlling reference station, and the final SOTF is established. When this occurs, the acquisition phase is complete and the synchronization phase begins. At this time, the TDMA terminal transmits all of its bursts according to the burst time plan, and adds traffic data to the short burst. The

final SOTF is such that the TDMA bursts are placed at their scheduled positions in the frame (plus or minus the synchronization error).

Terminals may have a dedicated acquisition window or they may share a common acquisition window. Terminals of the first type can perform acquisition in parallel; that is, two or more terminals can acquire at the same time. Terminals of the second type can only perform acquisition sequentially; that is, only one terminal can acquire at any one time.

Four sequential acquisition terminals can be acquired in one transponder, using a 16-control-frame superframe established for the TDMA system. The superframe is divided into four equal acquisition cycle intervals (ACIs) of three control frames each, separated by one control frame (guard space). Figure 6 shows the superframe structure. Each of the four sequential acquisition terminals is assigned an ACI, and can only perform acquisition during this time interval.

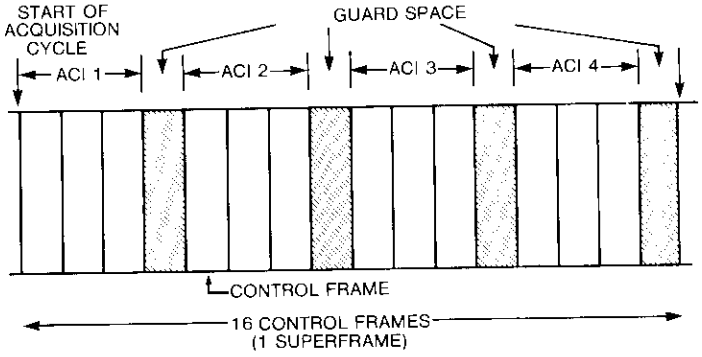


Figure 6. *Superframe Structure*

The terminal uses the CDC messages decoded from the reference bursts in a designated timing and control transponder to establish and maintain its transmit-side timing. These messages contain the transmission delay and the control code, as shown in Figure 7. Table 2 lists the four possible CDC control codes and describes their use.

The particular multiframe of the CDC control frame addressing terminal n is referred to as the control multiframe. When the terminal receives its control multiframe, it applies the decoded delay (and obeys the control code) for the first time at the beginning of its transmit multiframe, starting at time

$$t_K + 3T_M + D_n$$

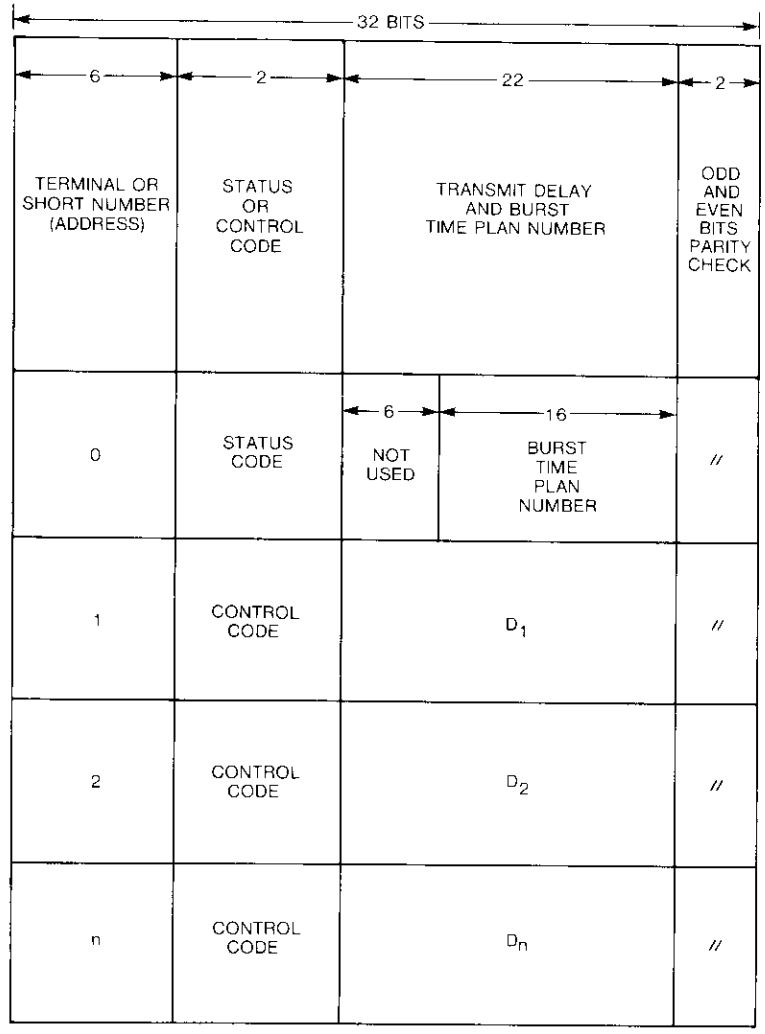


Figure 7. *Reference Burst CDC*

where t_K is the time of occurrence of the reference burst multiframe marker designating the beginning of the control multiframe of terminal n, D_n is the decoded delay, and T_M is the multiframe period (32 ms).

The particular transmit multiframe of terminal n in which the terminal first implements the newly received delay is referred to as the measurement multiframe. During this particular multiframe, the terminal transmits back

TABLE 2. CDC CONTROL CODES AND THEIR USE

CONTROL CODE	DEFINITION	REQUIRED ACTION
DNTX	Do Not Transmit	Do not initiate transmission. If already transmitting, terminate transmission.
IAP1	Initial Acquisition, Phase 1	Start transmission of short burst, if ready.
IAP2	Initial Acquisition, Phase 2	Short burst received at the controlling reference station (notification message).
SYNC	Synchronization Phase	Transmit all bursts (full traffic bursts).

its implemented delay via its SC. The controlling reference station(s) monitors a designated burst (principal burst) of controlled terminal n. When the measurement multiframe of terminal n occurs, the frame position of the principal burst is measured. The displacement of the measured burst from its scheduled frame position is subtracted from the previously implemented delay, and this new delay value is transmitted to the controlled terminal during its next control multiframe. Figures 8 and 9 illustrate these concepts. Figure 8 shows the terminal receive and transmit waveforms, and Figure 9 illustrates the burst position control mechanism by means of a time-space diagram showing the "trajectories" of the relevant multiframe markers.

Satellite position determination

The transmit delay for acquisition is computed at the reference stations based on knowledge of the satellite position and the geographical coordinates of the controlled TDMA station. This requires that an estimate of the current satellite position be continuously available at the reference stations.

Satellite position is determined at the reference stations by using either the satellite position prediction method or the real-time satellite position determination method. Satellite position prediction uses a mathematical representation (Bessel's polynomial expansion) of the satellite orbit, which is normally valid for a 24-hour period [3]. The precise satellite orbit is routinely computed in a mainframe computer in Washington from measurements performed by the INTELSAT TT&C stations. The coefficients of the polynomial expansion are obtained from the computed satellite orbit by means of a curve-fitting algorithm. These coefficients are transmitted via data lines to the reference stations, normally once a day but more frequently during satellite maneuvers.

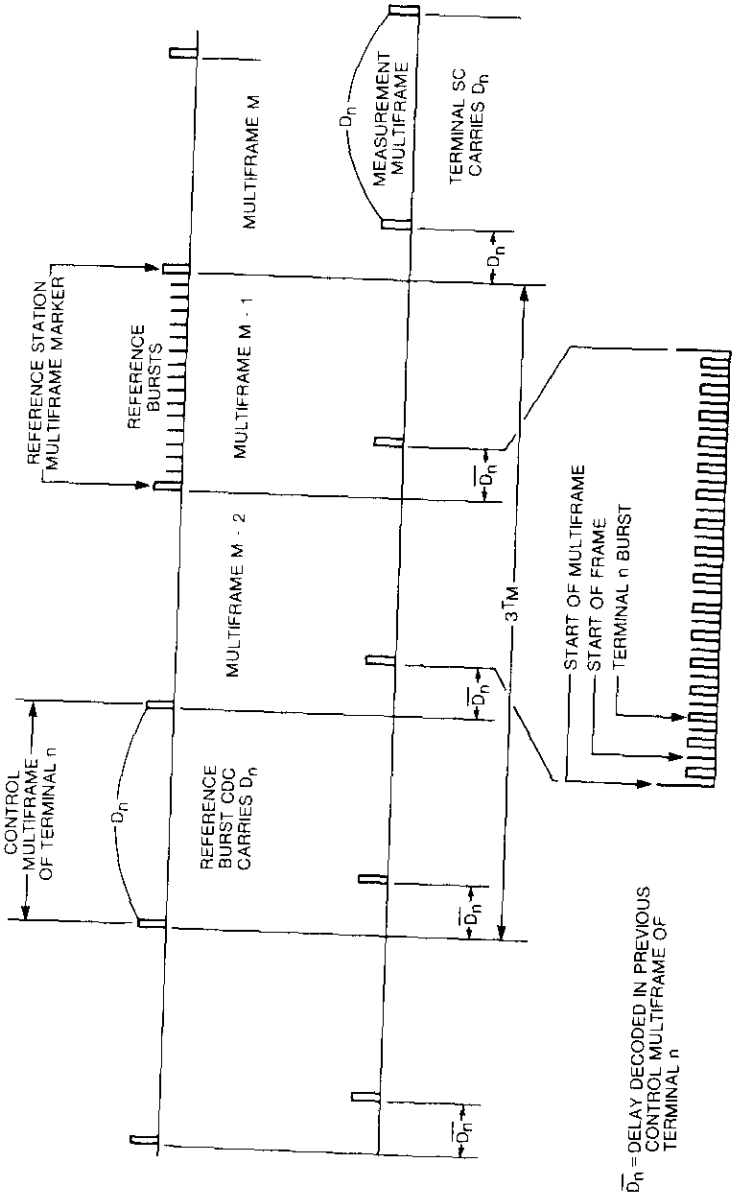


Figure 8. *Terminal n Control and Measurement Multiframes*

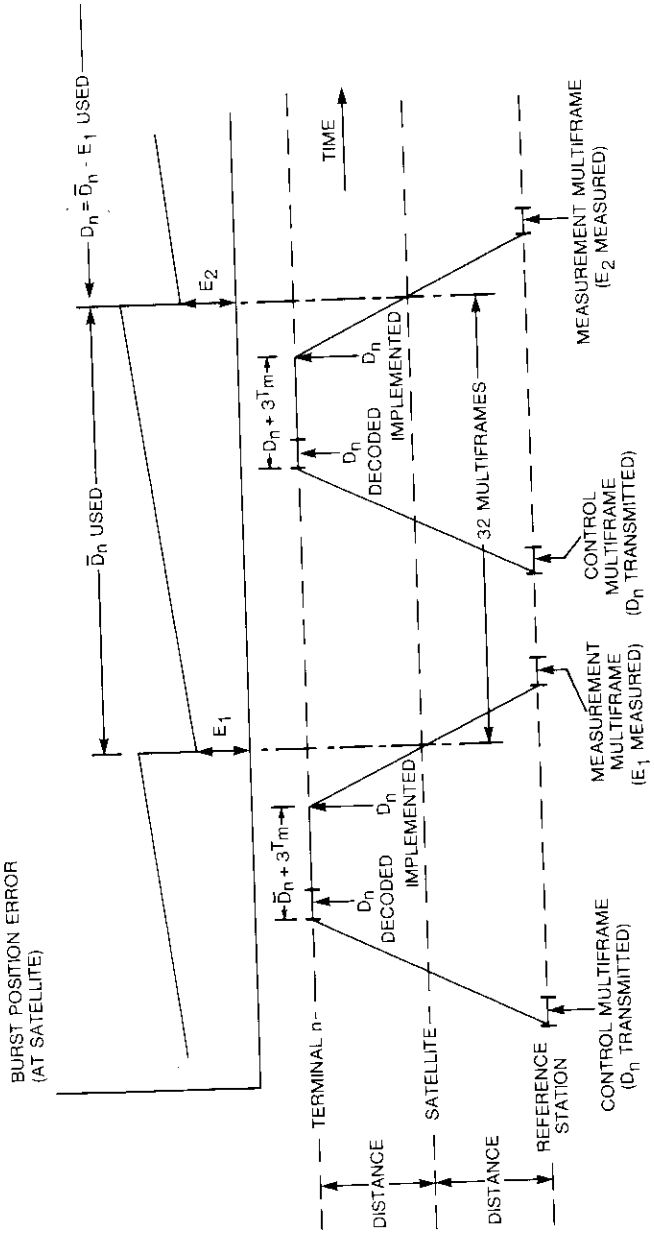


Figure 9. *Burst Position Control*

The local model of the orbit is used to compute an updated estimate of the current satellite position once every 16 seconds.

Real-time satellite position determination is a triangulation method based on measuring the distances between the satellite and geographically separated TDMA stations. These distances are measured by each reference station, with the cooperation of other TDMA stations. The cooperating station can be any controlled reference or traffic terminal. Two cooperating stations are sufficient when loopback connectivity is available; otherwise, three cooperating stations are required. The burst position control performed by the reference station provides the basic mechanism to compute the distance from the reference station to the controlled station via the satellite. When the required number of stations participate in the ranging process, the distances can easily be converted to the satellite position by using a triangulation algorithm.

Satellite position prediction will be the only method used in the initial phase of TDMA system operation, since well-separated ranging stations may not be available. In a mature TDMA system, when a good triangulation basis can be achieved, the real-time satellite position determination method will also be available.

System tests

Verification tests of the terminal acquisition and synchronization procedures have been performed on numerous occasions over the past few years, both in the laboratory and in the field [4],[5]. Two INTELSAT TDMA networks are currently operational, and a third is being tested. Considerable experience has been gained as a result of testing and implementation activities.

The basic acquisition and synchronization mechanism and its associated protocols have been proven to be sound, and no significant change in the original specifications was required. The burst position error measured during normal operation never exceeded 4 symbols (± 32 symbols are allocated for the worst-case synchronization error). Synchronization tests performed under severe link interference conditions (carrier-to-interference ratio in the 1- to 4-dB range) showed that synchronization was maintained.

Satellite position determination tests were also carried out using both the ranging method and the prediction method. The ranging (triangulation) tests, performed in a mixed hemi-loopback and zone-to-zone beam configuration, showed a satellite range error on the order of 1 km. This corresponds to a burst acquisition error of about 500 symbols ($\pm 2{,}500$ symbols are allocated for the worst-case acquisition error). The satellite prediction tests indicated that range prediction error did not exceed a few hundred meters when the satellite was not subject to maneuvers.

Tests were also performed during satellite maneuvers, and the results are shown in Figure 10. The prediction coefficients are based on an *a priori* estimate of the effect of the maneuver. After execution of the maneuver, the range error builds up (maximum observed value was 1.8 km). When new coefficients based on several hours of TT&C measurements were loaded into the prediction algorithm (after 1700 GMT) the range error decreased rapidly. After implementation of the final set of coefficients (based on 24 hours of TT&C measurements), a steady-state range error of less than 100 m was achieved.

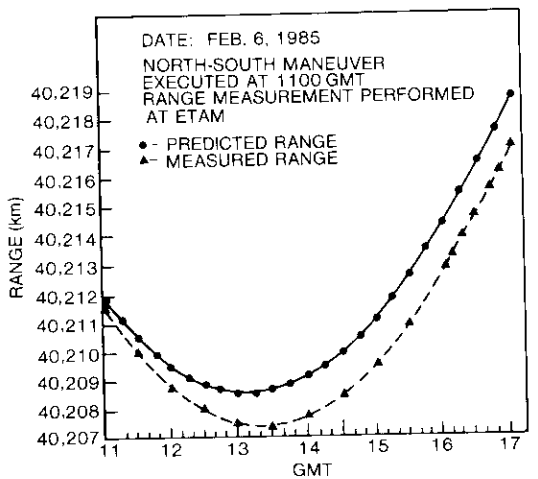


Figure 10. *Range Prediction Accuracy During Satellite Maneuver*

Conclusions

The basic principles of the terminal acquisition and synchronization approach implemented in the INTELSAT TDMA system have been described. The experience obtained in the testing and implementation phases of the TDMA networks indicates that the design objectives in the area of network timing have been met and, in many cases, exceeded.

Acknowledgments

The authors wish to thank the numerous individuals in INTELSAT and COMSAT, and the representatives of the INTELSAT Signatories, who participated in the development of the TDMA system specifications. A note of appreciation also goes to the industries which undertook the considerable task of converting these challenging specifications into working hardware.

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GianPiero Forcina graduated in Electrical Engineering from the University of Rome, Italy, in 1965, and performed postgraduate work at the George Washington University, Washington, D.C. Since 1968, he has been involved in the design of satellite systems both in Italy, at Telespazio, and in the United States, at COMSAT Laboratories, Fairchild Space and Electronics Company, and COMSAT General, where he was Manager of Systems Development. In 1978 he joined INTELSAT, Washington, D.C., where he has been largely concerned with the development of the INTELSAT TDMA System.

Roger Bedford received a B.Sc. in Electronic Engineering from Bolton Institute of Technology, England, in 1974, and an M.Sc. in Telecommunications from Essex University, England, in 1975. From 1975 to 1977, he worked on satellite system analysis and earth station design for the Marconi Company. In 1977, he went to Bell-Northern Research Laboratories in Canada, where he was involved in the integration of Canadian domestic satellites into the trans-Canada telephone network. In 1979, he joined Miller Communications System, Ltd., where he was responsible for system and hardware design of a 3-Mbit/s TDMA system.

Mr. Bedford joined INTELSAT in 1981, and has taken major responsibility for design evaluation, installation, and testing of the TDMA reference terminals. He is currently Principal Engineer in the Communications Engineering Department, and will be primarily responsible for evolution of the SS/TDMA system over the next 3 years.

Index: communication satellites, digital transmission, telephone transmission, speech processing, time division multiple access

Terrestrial interface architecture (DSI/DNI)*

J. H. RIESER AND M. ONUFRY

(Manuscript received November 15, 1985)

Abstract

The 64-kbit/s digital speech interpolation (DSI)/digital noninterpolation (DNI) equipment interfaces the time-division multiple-access (TDMA) satellite system with the terrestrial network. This paper provides a functional description of the 64-kbit/s DSI/DNI equipment built at COMSAT Laboratories in conformance with the INTELSAT TDMA/DSI system specification, and discusses the theoretical and experimental performance of the DSI system. Various digital terrestrial interfaces are examined for their effect on system design. Several DSI-related network and interface issues are discussed, including the interaction between echo control devices and DSI speech detectors, single and multidestinational DSI operation, location of the DSI equipment relative to the international switching center, and the location and need for Doppler and plesiochronous alignment buffers. The transition from 64-kbit/s DSI to 32-kbit/s low-rate encoding/DSI is expected to begin in 1988. The impact of this transition is discussed as it relates to existing 64-kbit/s DSI/DNI equipment.

Introduction

Speech signals occurring on telecommunications links are the product of two-way conversations. It is customary for one talker to pause while the

*This paper is based on work performed at COMSAT Laboratories under the joint sponsorship of the Communications Satellite Corporation and the International Telecommunications Satellite Organization (INTELSAT). Views expressed are not necessarily those of INTELSAT.

other speaks; thus, an active speech signal is present on a transmission channel for only a fraction of the available time. In addition, even when only one talker is speaking, pauses occur between utterances, so there are times when the circuit is idle. Measurements show that speech is present on a telephone channel approximately 35 to 40 percent of the time, averaged over a large number of busy trunks. Digital speech interpolation (DSI) systems exploit this low activity to reduce the information rate needed to handle a multiplicity of telephone speech channels [1].

INTELSAT has specified [2] a DSI system for operation with time division multiple access (TDMA) to serve a multinational community of users. This paper examines the design concepts and hardware complexities of this system, including performance characteristics and the effects of overload strategies and assignment protocols, in-band data signal performance, and the need for transmitting channels in a digital noninterpolation (DNI) mode. A variety of terrestrial interface issues are then discussed, concluding with some thoughts on the transition to the next generation of DSI systems.

DSI functional description

Functional block diagrams of a DSI encoder and decoder conforming to INTELSAT TDMA/DSI System Specification BG-42-65, including a data detector, activity simulator, and herding, are shown in Figures 1 and 2, respectively [3]. The INTELSAT DSI encoder and decoder are independent and derive their timing from associated TDMA frame clocks. As shown in Figure 3, a single DSI sub-burst is generated every 2 ms by each DSI encoder and consists of an assignment channel (AC) and a group of satellite channels (SCs). Each SC consists of 128 bits and is formed by 16 pulse-code modulation (PCM) samples of 8 bits each. The 128-bit AC is located at the beginning of each DSI sub-burst and carries three assignment messages used to route the terrestrial input channels to their destinations via the SCs.

Following the AC, there is a maximum of 127 SCs which can consist of a mixture of normal DSI SCs and preassigned DNI SCs. For a 127-SC system with both interpolated and preassigned DNI SCs provided, the preassigned DNI SCs occupy up to 15 of the highest ranking SCs without affecting the formation of overload channels.

When the number of terrestrial input channels that are active and in need of transmission exceeds the number of available normal SCs, least significant bits (LSBs) from the lowest ranking normal SCs are appropriated to form overload SCs, as shown in Figure 4. The LSBs from seven contiguous, normal SCs form one 7-bit overload SC. For the overload SCs, all of the most significant bits (MSBs) are transmitted first, the MSB-1 bits are transmitted

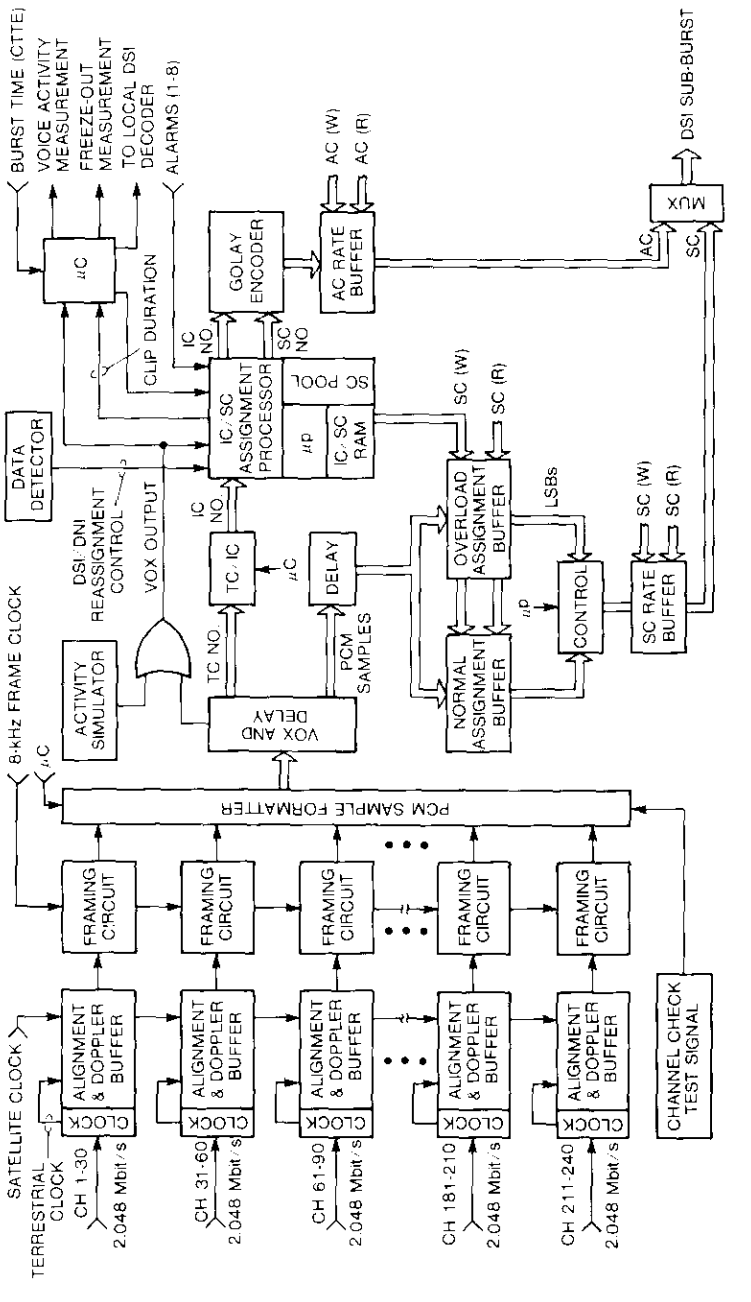

Figure 1. *DSI Encoder*

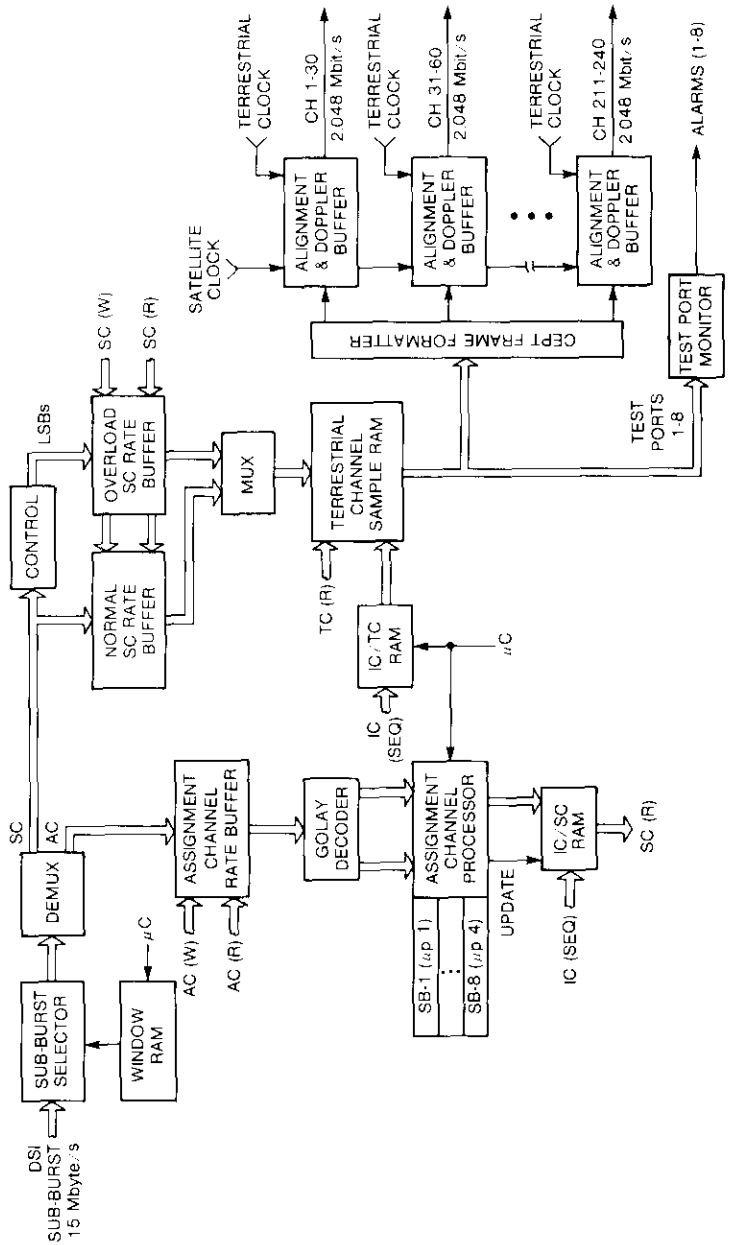

Figure 2. *DSI Decoder*

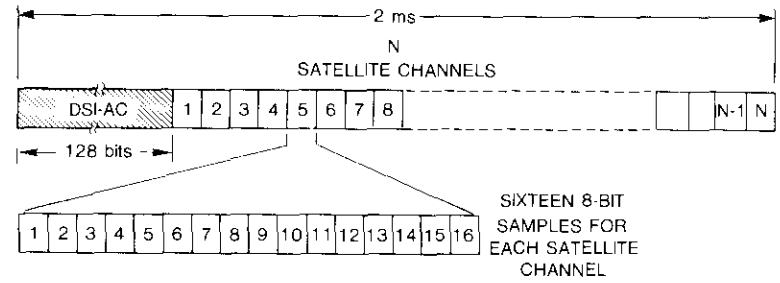

Figure 3. *DSI Sub-Burst Structure*

second, etc. For each overload channel, the seven SCs affected in this process remain normal, but contain only 7 valid bits. A maximum of 16 overload SCs can be formed from the first 112 normal SCs. For a DSI system operating with a maximum of 127 SCs, 15 are uninfluenced by overload channel generation and are available for preassigned DNI service. Use of additional DNI channels will reduce the maximum number of overload channels which can be formed.

Encoder description

Figure 1 is a functional block diagram of a 240-channel DSI encoder. The DSI input channels are derived from eight groups of 30 digitized 4-kHz telephone ports, each combined into a CEPT PCM serial line format at 2.048 Mbit/s.

Terrestrial interface

To accommodate the movement of the satellite and maintain a plesiochronous interface with the terrestrial network, each 2.048-Mbit/s serial input must pass through an alignment and Doppler buffer which retimes each of the eight CEPT PCM asynchronous inputs onto a single clock and performs a plesiochronous alignment of 125 μs (one CEPT frame). The Doppler buffer must have a capacity of 2.2 ms on both the transmit and receive sides to accommodate worst-case satellite path length variations. At the output of the encoder-side alignment and Doppler buffer, the eight serial CEPT lines are bit synchronous, but do not have a common frame relationship because of the arbitrary relationship among the phases of the read addresses in each of the buffers.

A framing circuit independently delays each serial line so it has a common frame relationship appearing at the input to the DSI encoder. At the output of the framing circuit, the serial lines are bit and frame synchronous and

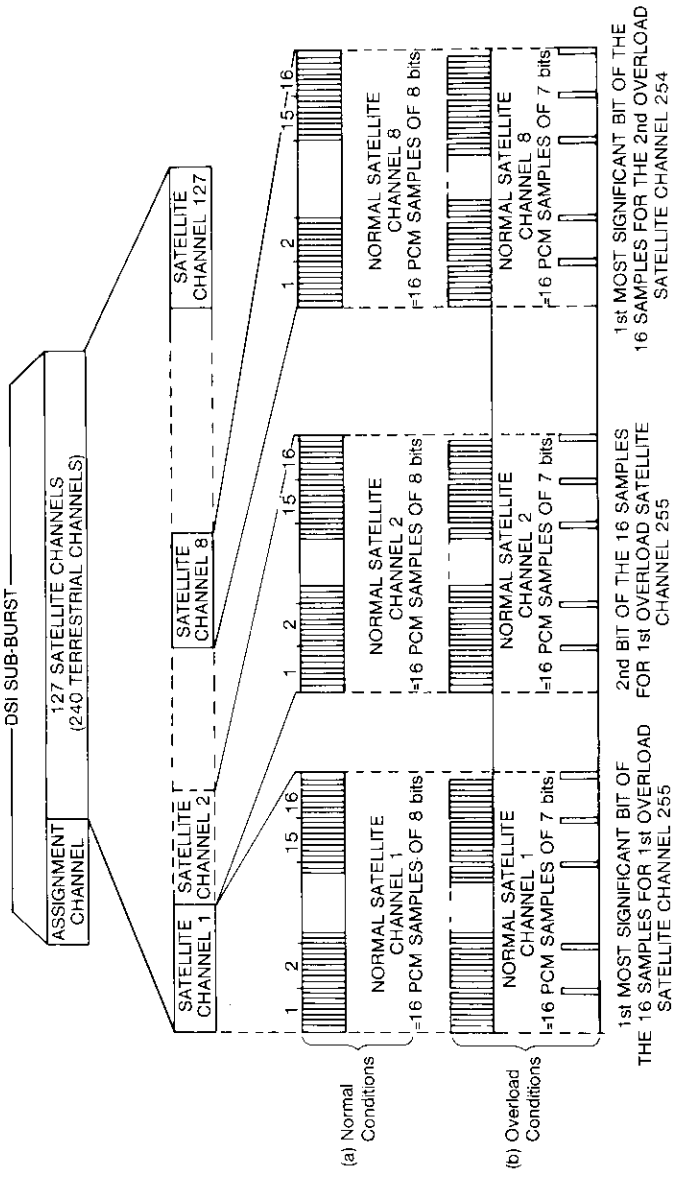

Figure 4. *Assignment of Satellite Channels in the DSI Sub-Burst*

thus properly timed for the PCM sample formatter. The alignment and Doppler buffers and framing circuits are unnecessary if the equipment providing the 2.048-Mbit/s serial input is driven with the TDMA/DSI system clock and frame clock.

DSI transmit-side processing

Figure 1 shows the PCM sample formatter which converts the 2.048-Mbit/s serial lines to 8-bit parallel samples, discards the synchronization and signaling time slots from the CEPT frame, and arranges the samples in ascending interface channel number order. A digitally generated channel check test signal is multiplexed into the 8-bit parallel output of the PCM sample formatter and competes with the active input channels for assignment to an available SC. The number of input interface channels is variable from 1 to 240 channels in single-channel increments and is controlled through the microcomputer.

The voice switch (VOX) is critical to the proper operation of the DSI system. Its major function is to recognize the presence of signals to be transmitted. As such, the VOX must be capable of discriminating between speech and noise over a wide dynamic range and must recognize speech quickly to avoid front-end clipping of the speech signal. To prevent excessive loading of the DSI system, the VOX must be immune to false activation on impulse noise, or if falsely activated it should only remain on for a short period of time. The BG-42-65 system specification permits the use of either a fixed threshold or an adaptive threshold VOX for detecting the presence of speech. The DSI terminal built by COMSAT uses an adaptive threshold VOX.

The VOX must also provide a measure of protection against excessive DSI loading which results from false detections on noise signals modulated by the echo control unit protecting the terminations. Excessive DSI loading will occur if the adaptive VOX threshold fails to track the modulated noise signal.

One method of minimizing excessive DSI loading is to allow the VOX to update the adaptive threshold at a rate which is high enough to track the modulated noise signal. A second method is to disable the threshold adaptation process when receive-side speech is present above an established level. This requires the receive-side speech control signal to have a hangover time of sufficient duration to match that of the echo control function. The noise modulation problem is not encountered by the fixed threshold switch; however, a fixed threshold switch can cause serious clipping on low-level speech signals and false activation on circuits with high noise.

The INTELSAT VOX specification incorporates the following features:

a. a fixed delay which minimizes front-end clipping by compensating for voice signal processing and DSI assignment message connection delay,

b. a floating detection threshold which increases the dynamic range and can be inhibited by receive-side speech, and
c. a variable hangover time based on voice spurt duration to minimize transmission of unwanted noise.

Although not part of the BG-42-65 system specification, a data detector independently monitors each input channel and alerts the assignment processor when voiceband data are present on the channel. Upon receiving a *data present* indication from the data detector, the assignment processor automatically reassigns the input channel from a DSI SC to a DNI SC for the duration of the data call. When data are no longer present on the channel, the assignment processor reassigns the input channel from a DNI SC back to a DSI SC.

Likewise not part of the BG-42-65 system specification, an activity simulator provides a means of artificially loading the DSI system so that performance can be measured for large, fully loaded configurations. Speech activity is simulated independently for a maximum of 240 channels. The simulated system size is controlled by the microcomputer and can be changed from 0 channels to 240 channels in 1-channel increments. The simulated channels can be used in conjunction with the actual input channels to provide artificial loading for a limited number of live test channels. The on/off speech spurt durations are modeled by exponential distributions which reside in read-only memory (ROM) and can be changed to suit particular loading requirements. A choice of two distributions, one for 35 percent and the other for 40 percent, is included in the present equipment.

Channel assignment processing

Each terrestrial channel (TC) is identified by an 8-bit binary number and translated by a programmable TC/international channel (IC) random access memory (RAM) into a corresponding 8-bit IC. The IC number and the VOX output state (active or inactive) are the primary inputs to the IC/SC assignment processor.

The assignment processor monitors the VOX activity state and various attribute registers such as SC type, pool status, and preassignment status for each channel and uses this information to route each IC number into either a new assignment, reassignment, or overload disconnect queue. A pool of available SCs is searched to find up to three unused normal SCs, three overload SCs, and three DNI SCs. An SC type may be omitted from the search if the programmed system configuration does not require its use. Once the SCs have been identified, three IC numbers are read from the queues and assigned to an appropriate SC. The queues are read in order of priority: new assignments first, reassignments second, and overload disconnects third.

When an IC becomes silent, the microprocessor locates the SC previously assigned to it and returns it to the SC pool to be used again. The assignment processor updates the IC/SC mapping RAM with each IC/SC relationship and also generates a corresponding assignment message. Three assignment messages are transmitted in each DSI frame. Since the capacity of the assignment message channel (1,500 assignment messages per second) is normally significantly larger than that needed to keep up with new voice spurt assignments even at peak load, there is ample opportunity to make frequent refreshments of previously made assignments.

The pools of available normal SCs, overload SCs, and DNI SCs are each independently variable in increments of one SC. This permits the number of SCs to be adjusted to achieve a desired DSI gain for any number of ICs served.

The assignment processor is implemented by a mix of hardware and software. High-speed hardware is necessary to search the SC pool for available SCs, and an 8-bit microprocessor is used to assign an available SC to each active IC and to update the IC/SC RAM and other status registers.

Provisions for sub-burst length modification

According to the BG-42-65 DSI system specification, once an IC has been assigned to a normal SC, the connection is held as long as the IC remains active unless a reassignment is requested. After an IC becomes inactive, the assignment processor holds the IC/SC connection unless a new connection or reassignment request for the SC occurs. Although this procedure provides circuit continuity under lightly loaded conditions, it encumbers simple methods of reducing sub-burst length since reassignments of continuing calls from higher numbered SCs to lower numbered SCs must be done either by manual intervention or by a special automated subroutine.

A *herding** process has been introduced into COMSAT's experimental 64-kbit/s DSI terminal that automatically assigns all ICs exhibiting speech spurt activity to the lowest numbered SCs independent of channel loading. This has the effect of concentrating the traffic at the beginning of the DSI sub-burst. Channels with continuously active signals are not reassigned and must be handled manually. Herding is particularly attractive when the DSI system interfaces directly to the common TDMA terminal equipment (CTTE), where burst length variation can be applied for traffic rearrangement. Active ICs can be automatically herded to the beginning of the sub-burst when burst time plan (BTP) changes require a reduction in the length of the DSI sub-burst.

*This function is not included in INTELSAT System Specification BG-42-65 [4].

Assignment map and SC transmission

The DSI system is configured and controlled through the peripheral CRT terminal and the resident microcomputer. System size, TC/IC relationships, IC/SC preassignments, and receive sub-burst identification are entered into the DSI system through the microcomputer, which monitors the ensemble speech activity and the freeze-out fraction and calculates a 1-minute average for each of these parameters.

Since an active IC can be assigned to any available SC, the DSI encoder must keep an up-to-date account of the IC/SC relationships for every terrestrial input channel. These relationships are stored in the IC/SC RAM and are referred to as a *map*, since they uniquely specify where input PCM samples are being routed. Once an available SC number has been obtained from the SC pool, it is used in conjunction with the IC number to update the IC/SC RAM. Each IC/SC assignment is Golay encoded and then entered into the AC rate buffer for transmission in the sub-burst.

The IC/SC RAM contains a unique map that is used to direct the PCM samples from a specific IC into a specific SC slot in either the normal or overload assignment buffer, depending on whether the map indicates that a normal or overload SC was chosen by the assignment processor. During the next frame, the PCM samples are written into the SC rate buffer from the normal and overload buffers. At this point, the LBSs of the normal SCs are replaced with the overload channel bits. The assignment processor controls the appropriation of LBSs for overload channel formation and allows bit reduction to continue on the normal SCs only as long as is necessary. During this same frame, the IC/SC relationships are read out of the AC rate buffer under the control of the CTTE. These relationships always precede the PCM samples by one TDMA frame and are used at the DSI decoder to process only those ICs destined for that station. During the next frame, the PCM samples relating to the previously transmitted IC/SC relationships are read out of the SC rate buffer under the control of the CTTE.

Decoder description

Figure 2 is a functional block diagram of a 240-channel, multidestinational DSI decoder. A TDMA terminal has the capability of transmitting up to 32 DSI or DNI sub-bursts in each 2-ms frame, but a DSI decoder is limited to receiving traffic from a maximum of 8 sub-bursts. The sub-burst selector performs prescreening, after which the received sub-bursts are demultiplexed to separate the ACs from the SCs.

DSI receive-side processing

The PCM samples carried in the normal and DNI SCs are written into the normal SC rate buffer, and the PCM samples in the overload SCs are written into the overload SC rate buffer. Both the normal and overload SC rate buffers serve as TDMA expansion buffers. The AC is written into the AC rate buffer and then Golay decoded.

Decoder assignment processor

The AC processor is implemented with high-speed hardware which screens the incoming IC numbers to be read by the DSI decoder. The IC numbers and corresponding sub-burst numbers designated for the decoder are entered into the AC processor through the microcomputer. An 8-bit microprocessor reads the assignment messages and updates the IC/SC RAM and other status registers.

Each DSI decoder has a list of originating ICs with which it corresponds. When an IC/SC message arrives at the DSI decoder, the SC is connected to the associated output port. Any prior connections to either the designated IC or SC are automatically disconnected. The receive-side connection is maintained until another IC/SC message reassigns either element of the association (IC or SC). When an IC/SC message is received at a DSI decoder for which the designated IC is not assigned, any connection to the designated SC is disconnected. Any assignment of an SC to IC 0 automatically disconnects all receive-side connections to that SC.

Each IC number designated for reception at a DSI decoder is translated by a programmable IC/TC RAM into a corresponding TC number, which is used in conjunction with the IC/SC RAM for routing SC samples into the TC sample RAM. The IC/SC map routes the contents of a particular SC into the TC sample RAM for each IC number associated with the TCs at the DSI decoder. Once the map in the IC/SC RAM has been updated, the DSI decoder directs the SC samples from the normal or overload SC rate buffer into the TC sample RAM, after which the PCM samples in these SCs can be read and formatted for standard CEPT transmission.

Conversion to CEPT format

The CEPT frame formatter converts the PCM samples from 8-bit parallel to serial format, arranges the 240 channels in 30-channel groups, and inserts an alternating synchronization word in time slot (TS) 0 and a dummy signaling word in TS 16. The eight CEPT serial outputs run at a 2.048-Mbit/s rate and are bit and frame synchronous with each other.

The serial data streams at 2.048 Mbit/s are each passed through an alignment and Doppler buffer to accommodate satellite movement and to

maintain plesiochronous operation with the terrestrial network. The serial data streams are independently clocked into the terrestrial network using the same clocks that were extracted from the corresponding serial input data streams at the local DSI encoder.

Channel check monitoring

The test port monitor measures the on/off durations of the channel check test signals originating from the eight corresponding DSI encoders, and compares the durations with fixed standards. If the on/off durations fall outside of acceptable limits, then the decoder signals the local encoder with an alarm, and the local encoder sends an alarm message back to the originating DSI encoder in the AC.

Digital speech interpolation performance

A 240-channel DSI system has 240 individual ICs which compete for a maximum of 127 normal SCs and 16 overload SCs. As described earlier, the 7-bit overload SCs are formed one at a time, as required, by appropriating the LSBs from seven contiguous normal SCs.

Overload processing

The overload SC numbers are used during periods of heavy input channel loading to reduce the occurrence of freeze-out, the temporary condition during which an IC becomes active but heavy demand leaves no SCs available for transmission. When freeze-out occurs, transmission is blocked for a short period of time and a speech clip occurs. The INTELSAT TDMA/DSI system performance objective requires that the DSI system operate with a sufficient number of SCs for each system size so that the probability of speech clipping in excess of 50 ms is less than 2 percent. This requirement was derived from Reference 5, which shows that for a 240-channel system, the 127 normal SCs and 16 overload SCs are more than sufficient to maintain INTELSAT-specified performance.

DSI system performance can be examined by plotting the freeze-out fraction and probability of a clip greater than 50 ms as a function of DSI gain [3]. The freeze-out fraction is the fraction of a talker's speech that is lost because no SC is available for transmission. DSI gain is defined as

$$\text{DSI gain} = \frac{\text{number of terrestrial input channels}}{\text{number of normal satellite channels}}$$

The freeze-out fraction, Φ_F, can be calculated from

$$\Phi_F = \sum_{i=\lfloor (8N/G)/7 \rfloor + 1}^{N} \binom{N}{i} \theta_t^i (1-\theta_t)^{N-i} \cdot \frac{i - \left\lfloor \left(\frac{8N}{G}\right)/7 \right\rfloor}{\theta_t \cdot N}$$

and similarly the probability, P, of a clip lasting more than 50 ms can be calculated from

$$P = \sum_{i=\lfloor (8N/G)/7 \rfloor + 1}^{N} \left[\binom{N-1}{i-1} \theta_t^{i-1} (1-\theta_t)^{N-i} \cdot e^{-iT/L} \sum_{j=0}^{i-\lfloor 8N/(G)/7 \rfloor - 1} \binom{i-1}{j} (e^{T/L}-1)^j \right]$$

In these expressions,

N = total number of terrestrial input channels
G = DSI gain
θ_t = (speech activity) × (channel loading)
T = 50 ms
L = average talk spurt = 1,350 ms
$\lfloor \cdot \rfloor$ = nearest lower integer.

Figures 5 and 6 show the freeze-out fraction and the probability of a clip greater than 50 ms as a function of DSI gain for various system sizes. These curves are used to derive DSI gain operating points. Originally, overload SC availability was not considered in the statistical calculations [5]. This special class of SCs was used to minimize the probability of speech clipping rather than to allow operation at higher DSI gains.

Figure 6 demonstrates that the present INTELSAT performance requirements can be met in a 240-channel system at DSI gains as high as 2.5, with an ensemble speech activity of 40 percent. This system configuration results in at least one overload channel being used 22 percent of the time. The fraction of time that any one channel encounters overload is less than this because of the randomness of the assignment process which spreads the impact of overload across all of the SCs. Alternately, for a 240-channel DSI system with a nominal DSI gain of 2, up to 21 percent of the 240 input TCs can carry continuous voiceband data (or be routed to a DNI channel within the DSI sub-burst), while the remaining voice channels continue to be

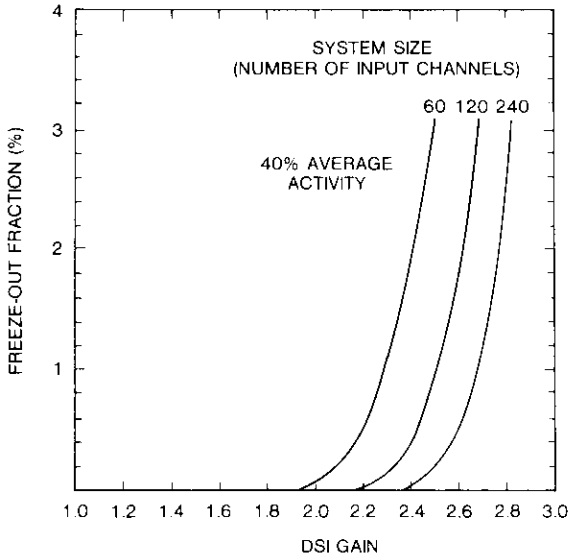

Figure 5. *Freeze-Out Fraction as a Function of DSI Gain for Various System Sizes [3]*

processed at a DSI gain of 2.5 and do not exceed the allowable probability of clip duration. Figure 7 shows the variation of DSI gain as a function of terrestrial input ports from 60 to 240 channels.

DSI baseband channel performance

The interpolation process influences the performance of the baseband channel during periods of overload. When 7-bit overload SCs are formed, the normal SCs carrying the overload SCs contain only 7 valid bits. If the number of active input channels exceeds both the number of normal and overload SCs, then the active channel must wait until an SC becomes available. Information lost during freeze-out is measured in terms of the freeze-out fraction, defined in BG-42-65 as the ratio of competitive clip duration to voice spurt duration averaged over all interpolated channels.

The performance of the DSI baseband channel with respect to the interpolation process and the TDMA link bit error rate (BER) was characterized during verification tests of the COMSAT 120-Mbit/s TDMA/DSI terminal [6]. A DSI baseband channel carried a 1.004-kHz test tone at 0 dBm0. At the DSI receiver, the test tone signal-to-noise ratio (S/N), C-message weighted, was measured with a distortion analyzer and recorded as a function of time on

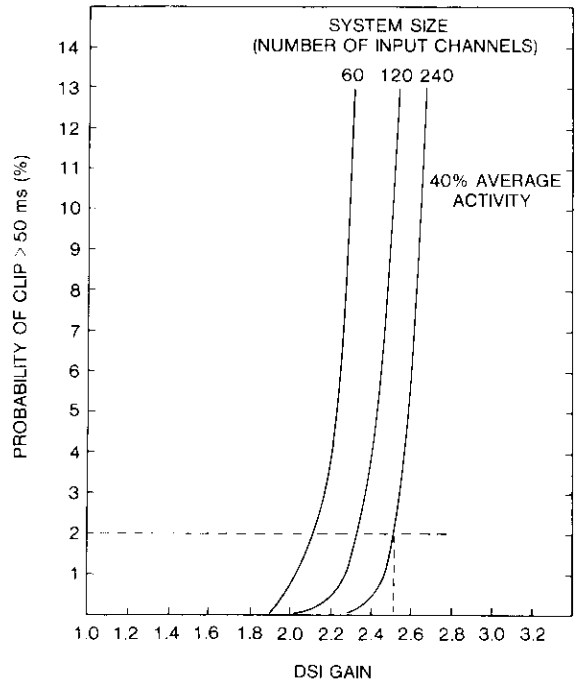

Figure 6. *Probability of Competitive Clipping > 50 ms as a Function of DSI Gain for Various System Sizes [3]*

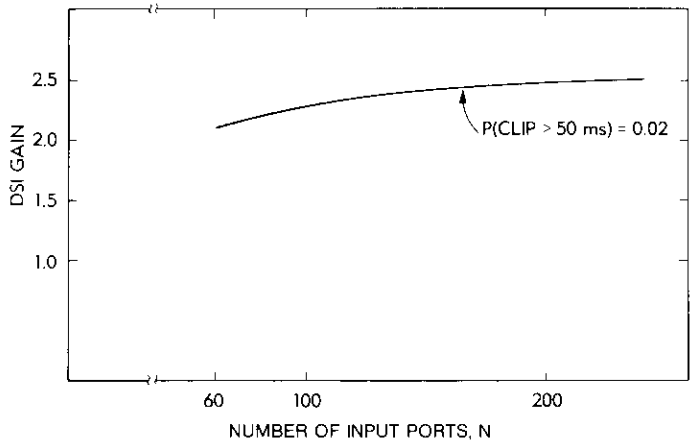

Figure 7. *DSI Gain as a Function of Input Ports [P(Clip > 50 ms) = 0.02] [3]*

an x-y plotter. The performance of the baseband channel was measured for the following operational conditions:

- 240 DSI input channels,
- TDMA channel BER of 1×10^{-6} and 1×10^{-4},
- DSI gain of 2.2 and 2.6, and
- forward error correction (FEC) off.

These tests were conducted with an activity simulator which provided the balance of the input signals. The average ensemble speech activity of the simulator was measured to be 42 percent.

Figure 8 shows the test-tone *S/N* plots, which indicate that increases in quantization distortion are directly related to increases in the freeze-out fraction and result from overload channels being formed from the LSBs of the normal SCs.

Echo control and DSI adaptive speech detector interaction

If the DSI system utilizes an adaptive threshold speech detector, interaction between the speech detector threshold adjustment and the echo control operation may generate excessive activity in the channel. The echo control device modulates the terrestrial circuit noise accumulated between the telephone and the send-input port of the echo control device. The adaptive threshold speech detector falsely classifies this terrestrial circuit noise as speech and increases the load on the DSI system. This will increase the occurrence of overload and freeze-out, thereby degrading the performance in the baseband channel. This interaction occurs as follows:

a. Receive speech arrives at the receive input of the echo control unit.
b. The echo suppression switch or canceller center clipper activates, stopping the echo and removing near-end-generated terrestrial noise.
c. If very little noise is generated between the echo control send-output port and the DSI speech detector input, the speech detector threshold will adapt to its minimum level.
d. When the receive speech stops, after a suitable hangover time, the near-end-generated terrestrial noise will return to normal as a step change in noise level.

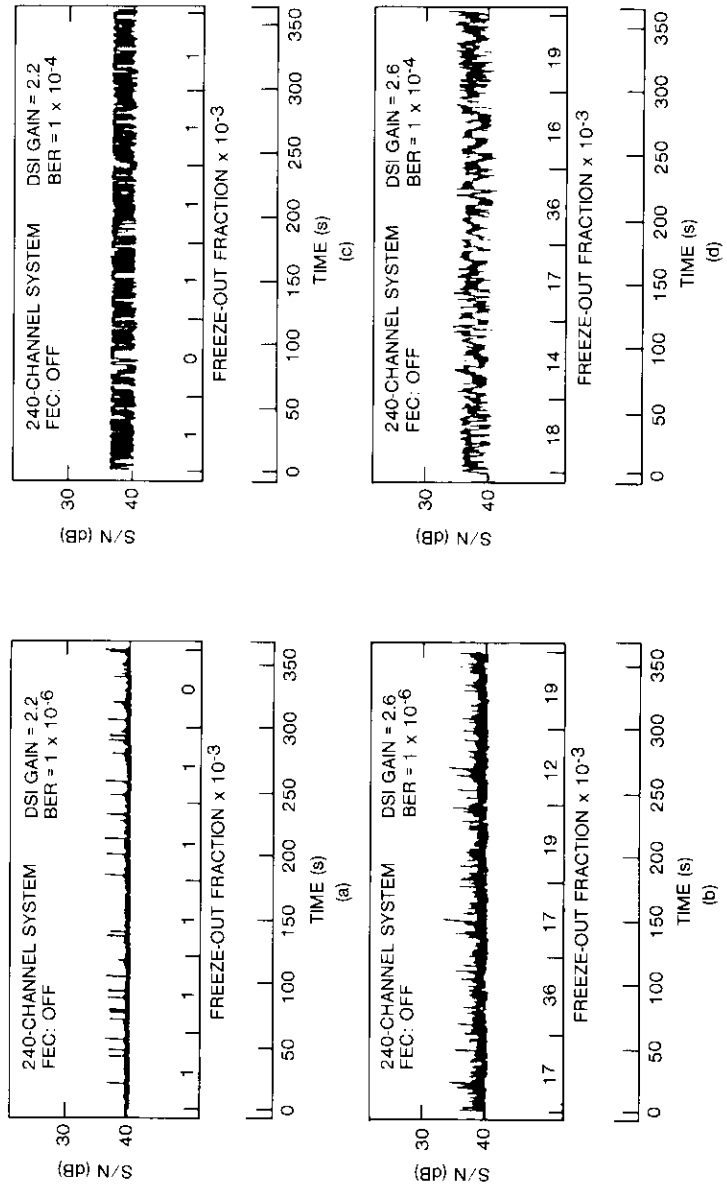

Figure 8. *Test Tone S/N and Freeze-Out Fraction vs Time*

e. This step change in noise level will exceed the speech detector threshold, causing the DSI system to transmit a noise spurt. The noise spurt duration will be a function of the adaptation speed of the speech detector and the near-end-generated terrestrial noise level.

This sequence will be repeated for every speech spurt and will produce a very annoying speech-correlated noise spurt heard by the talkers every time they stop speaking. There are several approaches to dealing with this interaction. In one approach, the echo control device can be modified so that it monitors terrestrial-generated noise at the send-input port. When the send transmission path is broken, noise at the proper level is injected into the send-output toward the DSI system, keeping the noise seen by the speech detector at a constant level and avoiding speech detector activation. In a second approach, a speech detector specification modification would be needed requiring the adaptive threshold on the transmit side to be frozen in the presence of speech on the corresponding receive channel. A third approach would be to specify an adaptive speech detector with a fast adaptation feature to minimize the noise spurts. However, specifying such a speech detector would require careful and extensive testing.

Digital noninterpolated channels

The INTELSAT DSI specification provides for the inclusion of DNI SCs within each DSI system to accommodate input signals, such as alternate voice data and direct digital data, that cannot tolerate interpolation and bit reduction. Several methods of implementation have been considered.

In a full 240/127-DSI system, the first 112 normal SCs can be used to form 16 overload SCs. This sub-burst structure leaves 15 normal SCs at the end of the sub-burst which are never subjected to bit reduction and can be used for DNI channel assignments. In this application, if one of the 15 SC numbers is chosen for DNI operation, it must be removed from the pool of SC numbers available for interpolation.

Reassigning channels from DSI to DNI accommodates an even larger percentage of DNI channels within the bounds of the sub-burst. The 15 SC numbers at the end of the DSI sub-burst can be used for DNI traffic, as described in the first method. However, as additional DNI capacity is required, the DNI slots progress into the DSI sub-burst at the expense of normal and overload SC numbers by eliminating the 16th overload SC number and using the seven normal SC numbers no longer subjected to bit reduction for DSI to DNI reassignments. These reassignments continue until the seven SC numbers are totally occupied by DNI traffic. At this point, additional DNI capacity can be accommodated by operator intervention, specifying the depth to which this process can continue to cut back into the DSI sub-burst. During periods of moderate DSI loading and high DNI activity, the sub-burst capacity is used very effectively. However, when DSI and DNI loading are simultaneously high, the DNI channels severely reduce the SC numbers available for interpolation, thus increasing the probability of a clip.

Redundancy and reliability

The DSI system must be highly reliable, but redundant equipment must still be available for automatic switchover in case of a malfunction. System redundancy could be provided by an on-line DSI system operating in parallel with each active DSI system. Both encoders would operate on the same input channels but share a common IC/SC assignment processor, SC pool, and IC/SC RAM. This interdependence would provide a smooth transition between encoders when a malfunction occurred. If the encoders did not share this common processing, the entire network could be disrupted at switchover because the IC/SC maps in the two encoders would be different. Likewise with the DSI decoder, the IC/SC RAM must be common to both decoders for a smooth transition to occur between decoders after a malfunction.

The INTELSAT DSI specification requires that system integrity be monitored by a continuous channel check test procedure which verifies channel assignments between DSI encoders and decoders by using an end-to-end continuity test. A test signal, consisting of a digitally derived 1-kHz square wave that is on for 1 s and off for 9 s, is multiplexed in PCM format prior to the VOX. This test signal competes with the other input channels for transmission in the sub-burst, and thus is subjected to interpolation, bit reduction, and possible clipping. The test signal is received at each of the corresponding DSI decoders and its on/off durations are continuously measured and compared with fixed standards. If the on/off durations fall outside of acceptable limits, an alarm message is sent back to the originating DSI encoder in the AC. The DSI encoder and decoder use these alarm messages to determine whether to switch over to the redundant units.

Digital terrestrial interfaces and their effect on DSI system design

Clock frequency differences which exist due to independent clock sources and the impact caused by satellite motion must be considered when interfacing to a satellite link. Motion compensation is a very important consideration in the satellite system because of path length changes which originate from an imperfect stationary satellite orbit. For a peak-to-peak path length variation

of 550 μs between the satellite and the earth station, compensation must be provided [7]. There are three basic ways of handling the timing of a digital interface: synchronous, asynchronous, and plesiochronous.

Figure 9 is a simplified representation of a digital interface between the satellite network and the digital terrestrial network. The digital interface exchanges data with both the satellite communications system and the terrestrial digital network and accepts a clock from both sources. Clock *S* (satellite) originates from the satellite communications system; clock *T* (terrestrial) originates from the terrestrial digital network.

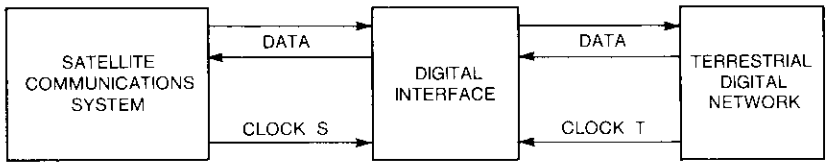

Figure 9. *Digital Interface*

Synchronous interfaces

If the *S* clock and *T* clock are the same, the interface is synchronous, as occurs when the terrestrial clock is derived from the satellite system clock. This case requires no processing at the interface. The synchronous interface is characterized by zero degradation, since there are no clock slips. If clocks *S* and *T* are locked in phase and frequency but have a fixed relative phase shift, resampling will normally accomplish the interfacing. In the more general case, clocks *S* and *T* may have long-term drift in relative phase, called *wander*, or short-term relative phase changes called *jitter*. The interface is still synchronous if the cumulative long-term time displacement between the two clocks is zero.

Buffering will be required in the synchronous interface if the peak-to-peak wander or jitter is greater than ½ bit. Except for magnitude, there is no fundamental difference between a wander of a few bits, as experienced in terrestrial systems due to clock drift, and the path length variation of thousands of bits, as experienced in geostationary satellite systems. The only requirement is that the buffer capacity be sufficient to absorb the path length variation.

Nonsynchronous interfaces

If clocks *S* and *T* are completely independent and nominally of the same frequency or different frequencies, the interface is referred to as nonsynchronous. Data flow across such an interface must be processed by either an asynchronous or plesiochronous operation in order to achieve continuous digital transmission.

ASYNCHRONOUS OPERATION

Achieving continuous data flow across a nonsynchronous interface by the asynchronous method involves the division of the input data stream into time-division multiplexed blocks, with bit synchronization re-established in each transmission block. The interface equipment must be designed for the specific block format to be used. The block boundary must be determined at the interface so that the required time adjustment can be absorbed in an idle period between blocks. This idle period is filled with dummy bits to produce what appears to be a continuous data stream by a method called *justification*. Justification can be used within the satellite system to compensate for Doppler, but cannot be used to solve the problem of the digital interface between the satellite system and the terrestrial digital network unless the data to be transmitted in the terrestrial network are formatted for justification.

First-order PCM multiplex structures (24- or 30-channel) do not have provision for justification as do higher order multiplex structures. The INTELSAT TDMA/DSI system does not presently support higher than a first-order multiplex level, and therefore justification cannot be used at this time.

PLESIOCHRONOUS OPERATION

Plesiochronous (meaning nearly synchronous) operation is defined for international digital links in CCITT Recommendation G.811.*

With reference to Figure 9, if clocks *S* and *T* are independent but each derived from oscillators of 10^{-11} accuracy, the interface is said to be plesiochronous. If the clock rate is 2.048 MHz and one clock is 1×10^{-11} high in frequency and the other 1×10^{-11} low, a time displacement error of 1 bit will accumulate in about 6.78 hours. In the case of the primary PCM multiplex structure defined in CCITT Recommendation G.732, it is suggested that slips be made in single-frame increments. Since a frame has 256 bits, frame slips will occur about every 72 days.

Location of the DSI system relative to the earth station

In a satellite communications network, the DSI system may be configured for single or multidestinational operation, with the optimum DSI system location influenced by the selected operating mode.

*All references to CCITT Recommendations refer to the *Yellow Book* approved by the VIIth Plenary Assembly, Geneva, November 10–21, 1980.

Selection of operating mode

Multidestinational operation of satellite systems permits any originating station's DSI transmission to be received simultaneously at all destination stations. Conversely, each destination can take traffic from all originating stations [8]. This feature is difficult to accomplish in terrestrial cable systems. Because an individual channel can be received from any one of several origins, all channels of a DSI frame must be received even if only one channel is designated for reception at a particular destination. This requirement places a heavy burden on the terrestrial facility between the earth station and a DSI receiver located at a remote switch.

For point-to-point or single destination operation, locating the DSI at the switch permits DSI capacity multiplication to be realized on the terrestrial facilities as well as on the satellite links. When the DSI is not colocated with the TDMA system, DSI frame synchronization (normally derived from the TDMA system) must be recovered by the DSI system at the remote switch location. This introduces additional complexity in accomplishing the synchronous BTP changes required by BG-42-65.

Design of Doppler/plesiochronous alignment buffers

Location of the DSI system relative to the earth station, and whether telephone traffic is delivered to the DSI system in analog or digital form, also impacts the design of Doppler and plesiochronous alignment buffers. The DSI system could be colocated at the earth station and interface to the terrestrial network in analog form, such as via a transmultiplexer. If the transmit- and receive-side analog-to-digital (A/D) and digital-to-analog (D/A) sampling clocks are independent, neither a Doppler nor a plesiochronous alignment buffer is needed. If the DSI system has only one clock for both the transmit and receive sides, then one Doppler buffer capable of absorbing path length changes on both the transmit and receive sides must be included, and it can be located on either the transmit or receive side. When the DSI system is colocated at the earth station and interfaced to a digital terrestrial link, a separate Doppler/plesiochronous alignment buffer must be located on both the transmit and receive sides.

The DSI system could be remote from the earth station. If it interfaces with analog terrestrial services and its A/D and D/A sampling clocks cannot be derived from the earth station clocks, then an independent clock must be used at the remote site, with the net result that separate buffers are required on the transmit and receive sides. If the remote clock is held to the 10^{-11} CCITT plesiochronous interface recommendation and Doppler/plesiochronous buffers are used, then frame slips will occur only once every 72 days. If the DSI system clock is held to an accuracy comparable to the Doppler variation of the satellite, or 10^{-8}, and only alignment buffers are used, frame slips will occur once every 104 minutes. When the DSI system is remotely located from the earth station and is interfaced to a digital terrestrial link, the DSI system runs on the terrestrial system clock and reflects this clock to the earth station. In this case, a separate Doppler/plesiochronous alignment buffer must be located on both the transmit and receive sides.

LRE/DSI transition

In an effort to improve channel utilization and reduce costs, a transition is expected from 64-kbit/s DSI to 32-kbit/s low-rate encoding (LRE)/DSI. The transition from 64 to 32 kbit/s will be dictated largely by system loading and the availability of LRE voiceband equipment. Implementation strategy will vary from user to user and will be a function of both the loading and the 64-kbit/s TDMA/DSI installation configuration at the earth stations involved.

A transition from 64- to 32-kbit/s voiceband encoding will provide a nominal 2-for-1 circuit multiplication factor and is the logical next step in increasing transmission system capacity. The recommendation by the CCITT of a standard 32-kbit/s voiceband encoding algorithm will accelerate equipment availability.

The 2-for-1 circuit multiplication provided by reducing the encoding rate from 64 to 32 kbit/s does not provide any increase in efficiency over that achieved by a 64-kbit/s TDMA/DSI network. Therefore, 32-kbit/s encoding is not expected to be implemented by INTELSAT unless DSI is used to provide an overall LRE/DSI gain of 4-to-1 and an increase by a factor of 2 over the channel multiplication provided by the 64-kbit/s TDMA/DSI. Those administrative and private operating agencies that provide a 32-kbit/s digital feed directly to the earth station may be exceptions.

Presenting a 32-kbit/s encoded signal to a DSI system produces new problems and imposes some constraints on system flexibility. Detecting speech on the 32-kbit/s encoded signal requires transcoding of the signal back to 64-kbit/s PCM prior to speech detection, or development of a new type of speech detector which operates on the 32-kbit/s adaptive differential PCM (ADPCM) encoded signal. Second, clips occurring in an ADPCM encoded signal cause the ADPCM encoder and decoder to mistrack, thereby creating a more serious problem than a clip in a PCM encoded signal. Therefore, it becomes important to avoid clipping the ADPCM encoded signal in such a DSI system, or to locate the ADPCM encoders so that any clipping occurs prior to ADPCM encoding.

Overload channel formation becomes difficult when the DSI system is operating on 32-kbit/s ADPCM encoded input signals. Formation of an overload channel requires that the 32-kbit/s input signal be transcoded back to 64-kbit/s PCM and then re-encoded as 24-kbit/s ADPCM. It is not possible to simply reallocate LSBs to form overload channels for an ADPCM encoded signal, as is common practice for a PCM encoded signal, because this would appear as a high BER to the ADPCM decoder.

It is likely that 64- and 32-kbit/s DSI systems will be colocated during the transition period, and they may be carried through the same TDMA system. The 32-kbit/s LRE/DSI can be interfaced directly with a TDMA CTTE port, as shown in Figure 10, thus simplifying the implementation of this equipment since proven 64-kbit/s PCM/DSI system designs can also be used for the 32-kbit/s LRE/DSI system.

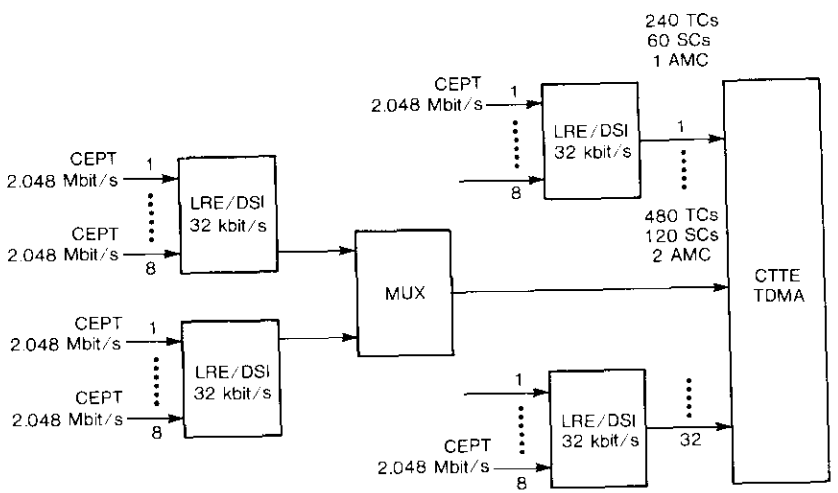

Figure 10. *Direct and Multiplexed LRE/DSI*

For a system configured to accept 240 input TCs, assuming a circuit multiplication factor of 4, only sixty 128-bit SCs would be required for a single LRE/DSI sub-burst. The sub-burst window required is one-half of that required for the transmission of 240 TCs with the standard BG-42-65 LRE/DSI system. During the transition period, both the 32-kbit/s LRE/DSI and the standard BG-42-65 DSI can be used, since each type can be interfaced with a separate CTTE port for burst transmission. The LRE/DSI can operate in single and multidestinational modes with other LRE/DSI units designed to the same specification. Some consideration could be given to modifying the CTTE to count out 64- rather than 128-bit SCs. However, if the 128-bit count is left in place, capacity growth in the LRE/DSI sub-burst would be constrained to increments of two ICs rather than the present one.

To handle the increasing requirements for TDMA terminal transmission capacity, either more sub-bursts will have to be accommodated, or twice the amount of traffic will have to be combined into one sub-burst by means of the specially designed multiplexer shown in Figure 10. This multiplexer will allow for a total transmission of up to 480 TCs in the same sub-burst window now allocated for 240 TCs, and is part of the DSI/CTTE interface not currently specified in BG-42-65. Thus, each administration would be free to implement this interface in a way that would be consistent with its current design.

Use of a direct interface has four advantages. First, it is fully compatible with the current TDMA system design. Second, integration of the LRE/DSI into the TDMA system will have little or no effect on existing operational traffic. Third, it can be used for single and multidestinational transmission between correspondents equipped with LRE/DSI systems designed in accordance with the same specification. And finally, two LRE/DSI outputs can be combined by a specially designed multiplexer for interface with one CTTE port, providing for transmission of up to 480 TCs per sub-burst and thereby improving CTTE port utilization.

Conclusions

The 64-kbit/s DSI system provides the TDMA network with a flexible and efficient interface to the terrestrial network in either a synchronous or plesiochronous manner. Designed to operate in either a point-to-point or multidestinational satellite environment, the DSI system should be colocated with the TDMA earth station equipment so as to minimize terrestrial transmission capacity in a multidestinational system configuration.

In a DSI system which utilizes an adaptive threshold type of speech detector, appropriate precautions must be taken in the design of the speech detector to prevent excessive channel activity from occurring because of the interactions between the speech detector and the echo control device. This excessive channel activity will increase the occurrence of overload and freeze-out, thereby degrading the performance in the baseband channel.

A direct-interface approach for transitioning from 64-kbit/s DSI to 32-kbit/s LRE/DSI operation has been discussed. It uses separate LRE/DSI units directly interfaced with the CTTE and is fully compatible with the current TDMA system design. Channel encoding at 32 kbit/s is not expected to be implemented by INTELSAT without DSI. The LRE/DSI system will provide an overall gain

of 4-to-1 and an increase by a factor of 2 over the channel multiplication provided by the 64-kbit/s TDMA/DSI system.

Acknowledgments

The ideas included in this paper have resulted from several years of effort involving a substantial number of people. Major contributors include S. J. Campanella and H. G. Suyderhoud, who have been actively working in the DSI area for a number of years. Their inputs and comments are greatly appreciated.

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Jack H. Rieser received a B.S.E.E. degree from the University of Cincinnati in 1975 and an M.S.E.E. from the Johns Hopkins University in 1982. He is currently a Staff Scientist in the Voice Band Processing Department of the Communications Techniques Division at COMSAT Laboratories. He was the Project Engineer responsible for the design and development of the INTELSAT BG-42-65 DSI terminal for use in the INTELSAT TDMA network. He is currently the Project Engineer leading the hardware development of a 32-kbit/s ADPCM/DSI system. Since joining COMSAT Laboratories in 1975, Mr. Rieser has had design and development responsibility for various DSI systems and speech detection devices. He also performed several studies in data and facsimile transmission via delta modulation at 32 kbit/s, and was the senior member of the team responsible for development of the first commercial COMSAT echo canceller. He is presently Chairman of the drafting group which is developing a DSI equipment standard in the U.S. T1Y1 Standards Committee. Mr. Rieser is a member of Eta Kappa Nu.

Michael Onufry received a B.S. degree from Pennsylvania State University in 1962, and performed graduate work at both Northeastern University and George Washington University. He is currently Manager of the Voice Band Processing Department in the Communications Techniques Division at COMSAT Laboratories. His experience includes echo canceller development, 64-kbit/s PCM and 32-kbit/s ADPCM, digital speech interpolation development, and encoding of speech. He has been active in planning and implementing international field trials in the INTELSAT network, and is responsible for subjectively assessing various speech processing devices. Since 1977, Mr. Onufry has been the COMSAT Representative to CCITT Study Group XV, where he has been a Special Rapporteur for questions concerning echo cancellers, syllabic companders, and digital circuit multiplication equipment. He is a member of IEEE, and past president of the Maryland Chapter of the ASSP.

Index: communication satellites, digital transmission, INTELSAT, synchronization, time division multiple access

A reference station emulator for testing INTELSAT TDMA/DSI terminals*

J. A. LUNSFORD AND T. R. DOBYNS

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Abstract

This paper describes the architecture and functional capabilities of a reference station emulator (RSE) developed for testing INTELSAT traffic terminal and reference terminal protocols and for verifying terminal performance. The RSE is basically a computer-controlled time-division multiple-access (TDMA) burst generator and burst receiver that has been specifically designed to test the traffic and reference terminals under both normal and stress conditions. Because the RSE can generate controlled fault conditions in reference and traffic burst stimuli, it can create specific stress conditions which enable detection of numerous protocol errors that would remain undiscovered with the use of simplified tests. Configurations for both laboratory and field tests are discussed.

Introduction

The reference station emulator (RSE) (Figure 1) is basically a computer-controlled time-division multiple-access (TDMA) burst generator and burst

*This paper is based on work performed under the joint sponsorship of the Communications Satellite Corporation and the International Telecommunications Satellite Organization (INTELSAT). Views expressed are not necessarily those of INTELSAT.

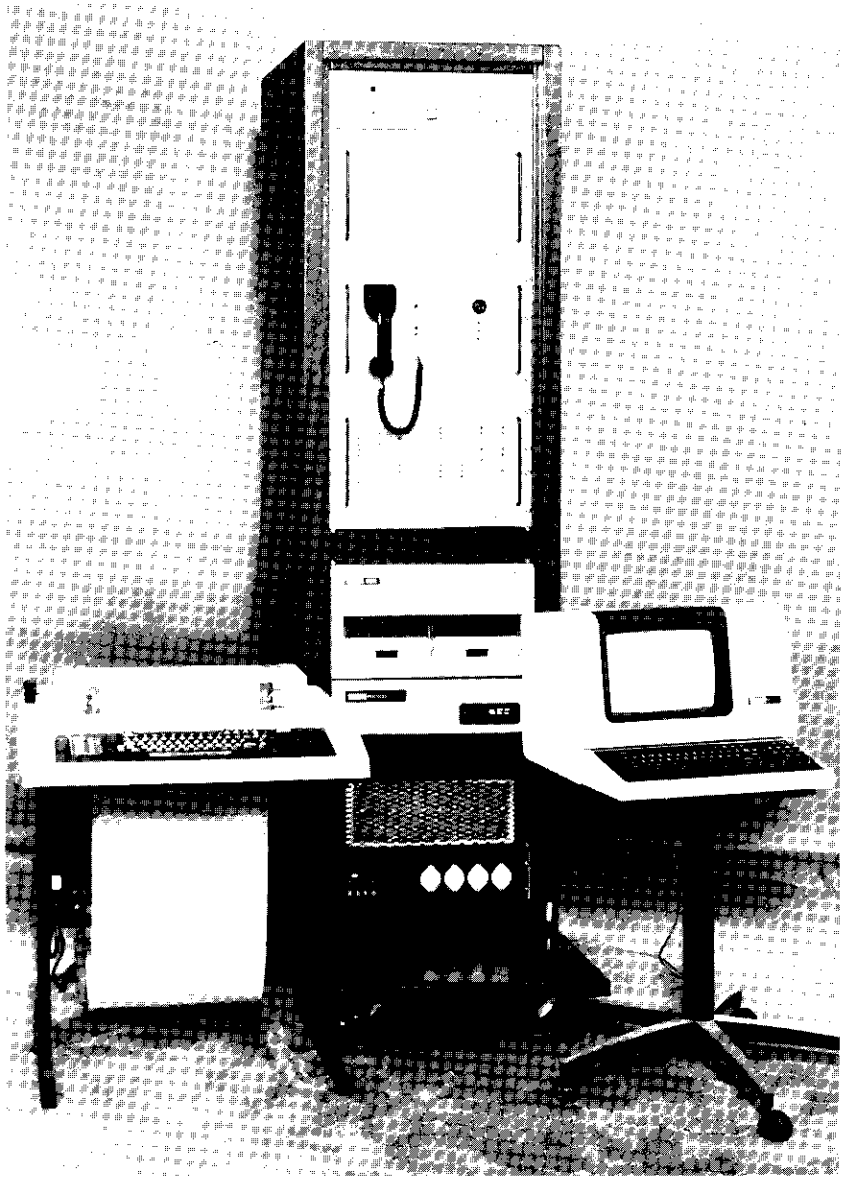


Figure 1. *Reference Station Emulator*

receiver that has been specifically designed to test traffic and reference terminals which are built to comply with INTELSAT 120-Mbit/s TDMA/digital speech interpolation (DSI) specifications. The RSE comprises a high-speed TDMA burst generator and receive unit which is similar to the burst controller in a TDMA traffic terminal, a pair of DEC PDP-11/23 computer systems that contain software for system configurations and test plans, processing routines for test results, and an operator station where commands are entered and results are displayed.

The RSE can be programmed to generate any or all of the following: reference burst 1 (RB1), reference burst 2 (RB2), and a traffic burst. The traffic burst may be the preamble only, or may contain the traffic portion of a receive traffic burst. The RSE can receive and demultiplex information from reference bursts and from up to three traffic bursts, measure the position of received bursts in the TDMA frame, and format a transmit delay correction value (D_n) for the controlled traffic or reference terminal to be sent in RSE-generated RB1 and RB2 bursts. The contents of all transmitted bursts (Figure 2) are also completely programmable. This allows test scenarios to be developed in which the three principal burst sections can be specified on a frame-by-frame basis. These principal burst sections are the unique word (UW), the control and delay channel (CDC), and the service channel (SC).

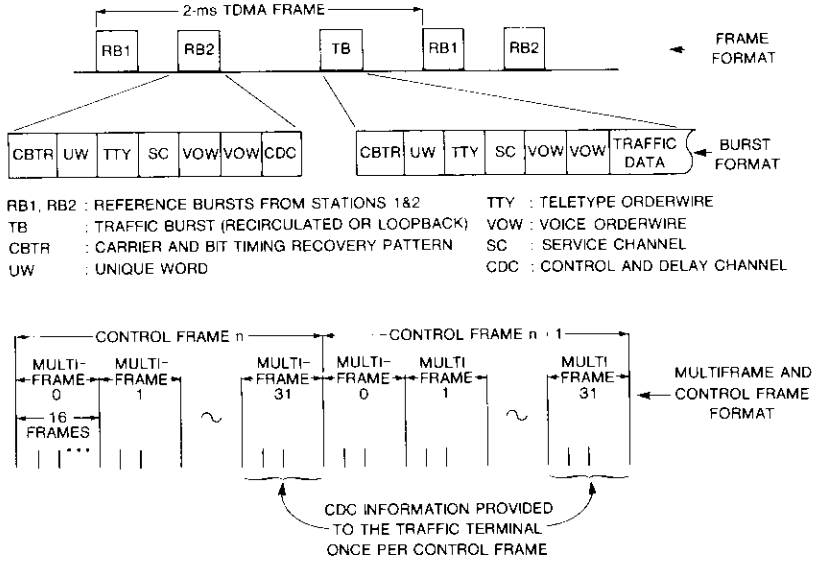


Figure 2. *INTELSAT 120-Mbit/s TDMA Frame and Burst Format*

The TDMA network synchronization and control system operates by using periodic variations in UW patterns to establish system timing markers and to identify RB1, RB2, and traffic bursts. The CDC contained in the preambles of the reference bursts is used to send acquisition and synchronization instructions to controlled terminals, and the SC contained in the preambles of both the reference bursts and the traffic bursts is used to monitor terminal status and disseminate system status information. The unique capability of the RSE to generate invalid and corrupted synchronization and control sequences, as well as valid and correct sequences, allows the development and execution of stress test programs to characterize traffic and reference terminals.

The RSE provides the following control functions on bursts, preamble, and data which it transmits:

a. Bursts

- generates two reference bursts,
- generates one traffic burst comprising a preamble only or a preamble and appended traffic,
- turns any burst on or off selectively, and
- controls burst position for any burst in the frame.

b. Preamble

- generates appropriate unique words for each burst (UW0, UW1, UW2, UW3),
- controls UW bit errors,
- controls UW frame alignment,
- controls the SC message in each multiframe of each burst,
- controls SC message parity, and
- controls SC redundancy errors.

c. Data

- controls the CDC message in each multiframe of each reference burst,
- controls CDC message parity,
- controls CDC redundancy errors, and
- selects received traffic data for retransmission in the RSE traffic burst.

The RSE controls its receive side in order to receive up to three bursts from a traffic terminal or one burst from a reference terminal. For each burst, the RSE measures burst position in each frame in a designated multiframe and counts UW misses each multiframe. The RSE reports these measurements to the RSE control computer once per control frame. In addition, the RSE reports the following information concerning the received bursts:

a. SC status message (number of losses per control frame and reason for loss of message, *i.e.*, UW miss, redundancy error, parity error),
b. received SC messages other than "ineffective message,"
c. "burst acquired/burst not acquired" condition of the burst, and
d. CDC content of a reference burst.

Design approach

The RSE has been designed as a general test instrument capable of providing comprehensive testing of INTELSAT TDMA/DSI traffic and reference terminal common TDMA terminal equipment (CTTE) equipment under both normal and stress conditions. Considerable attention has been given to providing the RSE with enough flexibility to extensively exercise almost every network timing and control protocol in both the reference terminal equipment (RTE) and traffic terminal equipment, and to generate controlled deviations that permit observation of terminal performance under such conditions. Because TDMA reference and traffic terminals are required to operate under various connectivities in the laboratory, the factory, or over the satellite in the network, the RSE has been designed to operate under all connectivity conditions.

Since a reference or traffic terminal responds to stimuli in the form of received bursts, the RSE has been designed to test terminals by generating TDMA bursts and observing the tested terminal's response (also in the form of TDMA bursts) to these stimuli. Normally, a TDMA terminal will receive TDMA bursts from a transponder containing two reference bursts and one or more traffic bursts. The terminal's protocols respond to the information contained in all of these bursts. The RSE provides two reference bursts and one traffic burst as stimuli in order to test all of a terminal's protocols, including a burst time plan change.

While it is certainly useful to verify that a terminal performs properly under normal conditions, the INTELSAT reference and traffic terminal protocols have been designed to protect the network when other than nominal conditions exist. It is also more valuable to verify that a terminal responds properly to fault conditions or conditions that deviate from nominal, since these conditions stress the terminal protocols and are more likely to induce serious protocol failures. It is also valuable to understand the failure mechanisms of a terminal before it enters the TDMA network, where the analysis of performance under abnormal conditions is quite difficult and may cause serious damage (*e.g.*, interfere with other terminals).

With this in mind, the RSE has been given the ability to program virtually any fault condition or sequence of conditions in any or all of its transmitted bursts representative of expected deviation from nominal. Bursts are programmed using a simple yet versatile assembly-like burst control language and an associated operating system for compiling and executing burst control programs to produce stimuli transmitted to the terminal under test. The programmer can generate control frame sequences of infinite duration, and has access to any bit in the UW, SC, and CDC of any burst in any frame, multiframe, or control frame in the sequence. With this capability, he can selectively program bits on data fields and add UW and redundancy corruption.

In order to observe and measure the tested terminal's response, the RSE has been provided with receive-side hardware which captures the terminal's transmitted bursts, measures burst position, and extracts SC data. If the tested terminal is an RTE, CDC information is also extracted. This information, as well as transmit data, is presented to the operator in well-organized visual displays. All the information transmitted and received is recorded in a data log to provide the capability for detailed analysis after a test is performed.

*Test configurations**

The RSE has the flexibility to accommodate many different test configurations, which can be grouped into the two general categories of laboratory tests and field tests.

Laboratory tests

The laboratory test category includes the following test configurations (shown in Figure 3):

- *Configuration A:* digital back-to-back tests.
- *Configuration B:* IF back-to-back tests.
- *Configuration C:* satellite link simulation tests.

Configuration A permits testing of the terminal response for different stimuli provided by the RSE, while Configuration B permits the same tests to be performed in the presence of additive noise. Configuration C permits

*R. Ridings *et al.*, "Verification Tests of a Prototype INTELSAT TDMA/DSI Terminal," Sixth International Conference on Digital Satellite Communications, Phoenix, Arizona, September 1983, *Proc.*, pp. II-14–II-23.

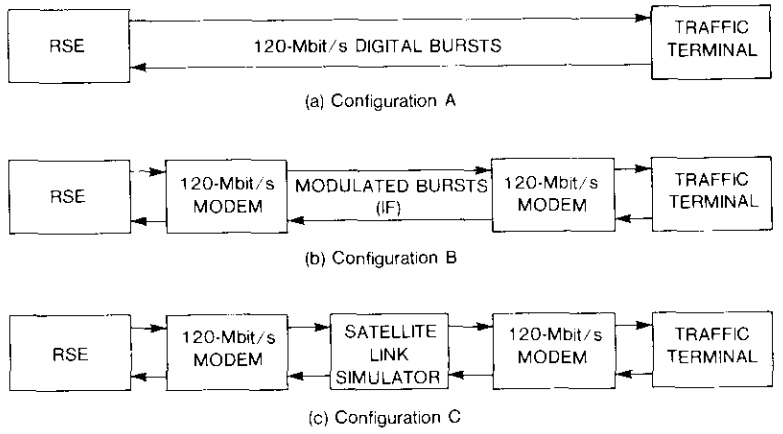


Figure 3. *RSE Laboratory Test Configuration*

simulation of the network over a satellite link, including linear and nonlinear channel distortion, thermal noise, and interference.

In Configurations B and C, the link bit error rate (BER) can be measured using the traffic data recirculation feature built into the RSE. This feature permits the traffic data contained in one received traffic burst to be extracted, and a new traffic burst containing the same data to be generated by the RSE. The BER of the retransmitted traffic data can then be measured by the originating traffic terminal.

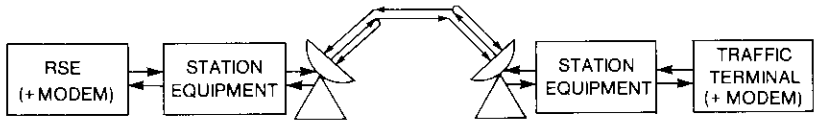
Field tests

Under the category of field tests, two configurations are identified (see Figure 4):

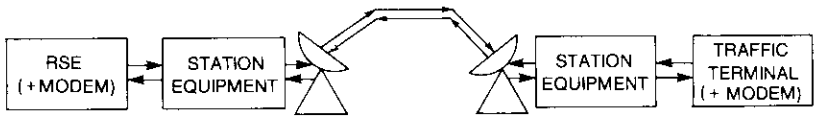
- *Configuration A:* loopback connectivity.
- *Configuration B:* beam-to-beam connectivity.

In Configuration A, both the RSE bursts and the tested terminal bursts are transmitted in the same frame and received by both the RSE and the tested terminal. The RSE has the capability to synchronize its receive timing to the reception of its own burst. In addition, the RSE can control the tested terminal's transmit timing so that its bursts are kept in a preassigned location in the frame. These two features permit the RSE to simulate the operation of an actual reference terminal.

In Configuration A, the procedures of the test terminal can be examined under normal and stress conditions (simulated by the RSE) over the actual



(a) Configuration A



(b) Configuration B

Figure 4. *RSE Field Test Configuration*

satellite link. Stress conditions are abnormal conditions such as loss of primary reference burst, secondary reference burst, UW, and CDC channels. The TDMA network control procedures are robust in the sense that these abnormal conditions can be tolerated for a reasonable time, during which the network and TDMA terminals continue to operate. Testing under simulated stress conditions verifies that a terminal will operate under abnormal conditions as required.

In Configuration B, neither the RSE nor the traffic terminal receive their own transmitted bursts. In normal operation, a TDMA frame contains at least one reference burst; however, in Configuration B the TDMA frame received by the RSE contains only a traffic burst. The RSE has been designed to operate in this nonstandard mode in order to test a traffic terminal in a zone-to-zone configuration. Without this feature, a second RSE, or an RTE, would be required. To operate in this configuration, the RSE maintains the position of the received traffic burst aligned with the RSE transmit frame. Since the TDMA frame received by the traffic terminal appears as a normal TDMA frame, the traffic terminal is unaware that it is being operated by the RSE. All protocol tests can be performed in this configuration, and the RSE can recirculate the received traffic burst data in the RSE traffic burst to permit end-to-end traffic channel testing.

RSE hardware description

Figure 5 is a functional block diagram of the RSE hardware. The functional elements can be categorized as follows:

- control functions,
- transmit functions,
- receive functions, and
- interface and configuration functions.

Control functions

The RSE control functions are implemented by the control computer and direct memory access (DMA) buffer illustrated in the figure. The control computer generates all the information contained in the UW, SC, and CDC of each transmitted burst, as well as burst corruption information. This control information is organized by multiframe into a control frame data block, and is transferred to the DMA data buffer once per control frame (1.024 s) by DMA transfer. A control frame consists of 32 multiframes, each controlling a different terminal, with sixteen 2-ms frames per multiframe.

The data buffer is accessed once per multiframe by the transmit control hardware in order to obtain the data required to generate the next transmit multiframe. The control computer also receives burst measurement information from the receive-side hardware for interactive program control, storage, and display on the operator interface.

The control computer shown in Figure 5 comprises two DEC PDP-11/23 computer systems. One computer performs program generation and control functions, while the other performs message processing, data storage, and

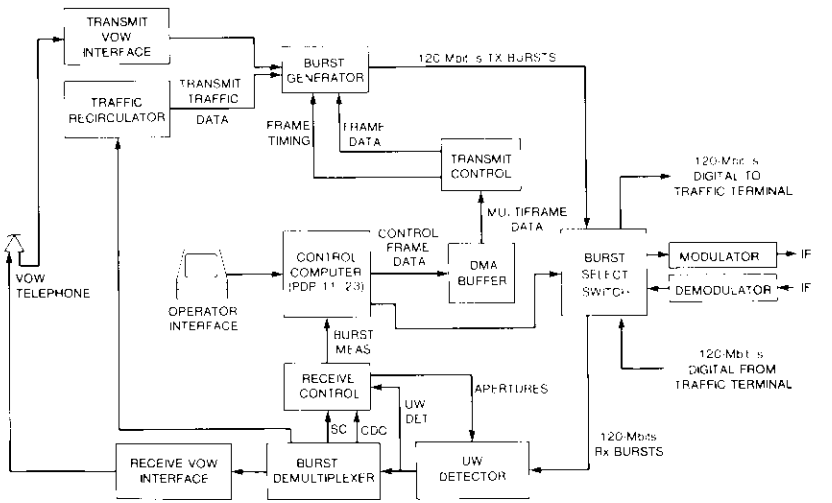


Figure 5. *Functional Block Diagram of the RSE*

display functions. Each computer provides input/output to a video terminal. The RSE may be controlled from either terminal; however, program generation can only be performed from the control computer terminal.

Transmit functions

The transmit functions are implemented by the transmit control, burst generator, and traffic recirculator. The transmit control contains a flywheel timing generator which generates multiframe and frame timing instants. At the beginning of each multiframe, the transmit control presents multiframe data processed in the previous multiframe to the burst generator at frame intervals (*i.e.*, every 2 ms). This information consists of the CDC and SC bits and the UW for each burst in each frame of the multiframe, along with relevant corruption information. In addition, the transmit control reads the next multiframe's data from the DMA buffer and processes these data in preparation for the next multiframe interval.

The traffic recirculator receives one sub-burst of data from one of the received traffic bursts and stores it for retransmission. The burst generator formulates the reference and traffic bursts from the recirculated traffic data. Bursts are generated relative to the start-of-transmit frame (SOTF) provided by the transmit control at a time specified in the transmit burst time plan. It should be noted that the RSE transmit timing is provided by a flywheel generator and is not controlled by a value of transmit delay, as in a normal traffic or reference terminal. Consequently, the RSE's bursts are generated as in a master primary reference terminal.

Receive functions

The receive functions illustrated in Figure 5 are implemented by the receive control, UW detector, and receive burst demultiplexer. The receive side is essentially the same as that of a traffic terminal, except that it is capable of performing burst position measurement of received traffic and reference bursts. The receive control generates a start-of-receive frame (SORF) based on either internal timing derived from the RSE-transmitted reference bursts or on the reception of reference bursts (its own transmitted bursts, or those of an RTE). This SORF, along with burst location data contained in the receive burst time plan, is used to generate apertures during which the UWs of received bursts are detected.

The receive control compiles information concerning the status of the bursts received from the test terminal, including number of UW losses per multiframe, cause of SC message loss, and burst position error. The receive control then passes these data to the message processing and display computer. The UW detector performs correlation detection of the received bursts, gates the correlation spike within the UW detection aperture, and passes these detected pulses to the receive control and burst demultiplexer.

The burst demultiplexer extracts the SC and CDC or traffic data from received reference and traffic bursts. SC and CDC data from reference bursts are provided to the receive control. The traffic data from a designated receive traffic burst are provided to the traffic recirculator, and traffic data from other traffic bursts are ignored.

Interface and configuration functions

The RSE's capability of providing fully variable control stimuli to traffic terminals is achieved mainly through the complex software that supports the operator interface. This software operates in the RSE control computer and allows the operator to create, modify, and execute RSE control programs. These operator-generated programs are processed by the control computer to determine the control data for the various microprocessors within the RSE hardware. The control data are generated once per control frame and are basically memory maps that control the transmission and reception of bursts, burst contents, and RSE configurations. In addition, the state of the RSE hardware is monitored to provide input data for the control programs, thus allowing emulation of interactive, decision-based reference terminal equipment procedures.

An RSE test program consists of three major component specifications: RSE configuration, burst content, and burst positioning. For the RSE to properly execute a test program, each component must be defined. Since the configuration and the burst positioning specifications will generally be the same from test to test, a unique test is usually the result of a unique burst content specification. However, certain tests may require the same burst content but different connectivity, and thus a different configuration.

Figure 6 illustrates the relationship between the general specifications mentioned above and the RSE system. Each specification is entered by the operator via a separate handler. The RSE configuration handler is contained within the RSE monitor program. The other two handlers are stand-alone programs which execute on the RSE control computer.

As indicated in the figure, the output of each specification handler is a disk-based data file containing assembled code. Each specification handler may access its respective disk file and modify it or use it to create a new disk file. With the exception of the configuration data file, all files are accessed by file name.

When an RSE test program is executed, the RSE monitor accesses the data files identified by the operator. The monitor records the filename of the last identified file upon execution. If the operator executes without identifying

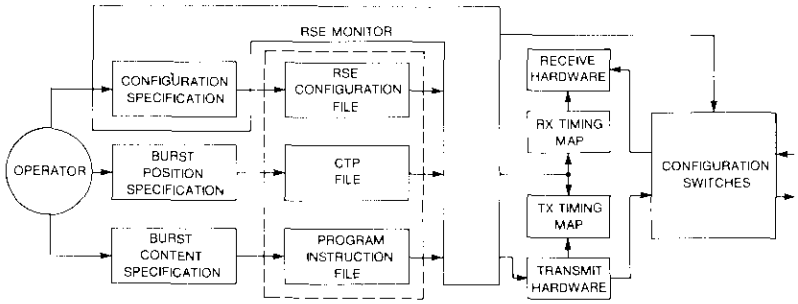


Figure 6. *Relationship Between Test Specifications and Their Function in the RSE Hardware*

one of the data files, the monitor automatically looks up the name of the last file executed and accesses that data file. This feature greatly simplifies the operator interface, especially when a particular test is executed repeatedly.

As shown in Figure 6, the contents of the RSE configuration data file are used by the hardware configuration switches to program the RSE to be in one of the test configurations described above. The data file also contains parameters pertaining to the type of terminal being tested (RTE or traffic terminal). The burst position specification generates a condensed burst time plan (CTP) data file containing information about the location of transmit and receive bursts in the TDMA frames. The data are down-loaded into the RSE transmit and receive timing maps upon system reset. The timing maps are used by the transmit and receive timing controls to locate bursts in the TDMA frame.

The burst content specification generates a data file containing instructions used to program the information content of transmitted bursts. Because the refresh rate of the microprocessors in the RSE hardware is once per control frame, RSE control programs are constructed so that the contents of a single control frame are always fully defined. This is known as the control frame data block, and is sent to the RSE hardware once every second. Creation of a burst content specification (control program) proceeds by first defining the base control frame segment of the program, which defines completely the contents of the control frame data block at the start of the program. This base control frame is modified by defining up to 32 change elements in which one or more attributes of the base control frame are changed. Thus, up to 32 different types of control frames may be defined within a control program.

The final step is to write the program flow segment, which determines the order and conditions under which the change elements are invoked. This may be a simple routine, such as a count of transmitted control frames, or it may be interactive with a tested terminal's response; that is, it may examine

incoming (traffic terminal) burst status and switch the transmitted control. In addition to controlling application of the change elements, the control program can be placed under manual control for selected events or conditions. In this mode, the operator can either modify the control frame contents or continue control program execution from different entry points.

The change elements consist of one or more mnemonic-type statements called *change instructions* which specify the required modification to the contents of the control frame data block. The functions listed in the introduction can be programmed by using these change instructions.

Example of test application

This section describes a simple test to verify the flywheeling capability of the receive-side protocol of the traffic terminal. In particular, this test verifies that the steady-state reception (SSR) procedure operating on the received reference burst(s) continues to operate (on internal timing) when the received reference burst(s) is lost for less than 512 consecutive frames. Test Configuration A in Figure 3 was selected; however, the return data link (from the traffic terminal to the RSE) was not implemented.

The test sequence listed in Table 1 is programmed into the RSE so that the correct response of the terminal can be readily confirmed from visual observation of the front panel indicators which show the state of the terminal. The test sequence repeats every 10 control frames, which is approximately

TABLE 1. RSE TEST SEQUENCE FOR SSR TESTS

CONTROL FRAME	MULTIFRAME	REFERENCE BURST FRAME	REFERENCE BURST STATUS*	REMARKS
1–3	1–32	1–16	On	Normal operation.
4	1–31	1–16	Off	511 losses.
4	32	1–15	Off	
4	32	16	On	4 detections.
5	1	1–3	On	
5	1	4	Off	
5	1	5–16	On	
5	2–32	1–3	On	
5	2–32	4	Off	Loss of third UW after multiframe marker.
5	2–32	5–16	On	
6–10	Repeat control frame 5 sequence			

*One reference burst per frame is transmitted in this test sequence.

every 10 seconds. The underlying structure of the test is as follows. The reference burst is present in each frame of the first three control frames, which is ample time for the terminal receive-side protocol to locate the burst and declare it reliably received, or "burst acquired." The SSR procedure continuously checks that the conditions for declaration of reliable reception of the burst still apply; otherwise, "burst not acquired" is declared.

The flywheeling capability of the SSR procedure permits continuation of the "burst acquired" declaration, even if the reference burst has been lost for each of the previous 511 frames. To test this capability, the reference burst is turned off for the first 511 frames of control frame 4, and turned on again for four additional frames. According to the SSR specification, this should not result in the "burst not acquired" declaration. In the rest of the test sequence, the reference burst is on, except in the fourth frame of each multiframe. This is done to facilitate visual observation of the "burst not acquired" status on the terminal front panel should this condition be erroneously declared after 511 consecutive burst losses. In this case, the missing burst in the fourth frame of each multiframe would inhibit reacquisition of the burst, thereby causing the "burst not acquired" status to be displayed for approximately 6 seconds, which is sufficient time for observation.

This test was successfully performed on a prototype traffic terminal built at COMSAT Laboratories. It is an example of one simple test. Many other more elaborate test sequences have been designed for testing different traffic terminal protocols.

Conclusions

The RSE developed to test INTELSAT reference and traffic terminal CTTE has been described. The RSE was used to comprehensively test a prototype TDMA terminal built by COMSAT Laboratories, and to verify that the terminal complied with INTELSAT TDMA/DSI Traffic Terminals Specification BG-42-65, Rev. 2. This terminal had previously been tested using a simplified test set which provided only normal reference burst stimuli. During testing with the RSE, numerous protocol errors were found which were not detectable using the simplified test set. This is attributable to the RSE's ability to generate controlled fault conditions in the reference and traffic burst stimuli. A comprehensive set of generic protocol tests capable of testing the function of a traffic terminal completely and expeditiously is currently being written.

As a burst generator for TDMA terminal development, the RSE is unparalleled. It is capable of testing a large portion of the reference terminal protocols, including terminal acquisition and synchronization support procedures. Additionally, its ability to stress-test a terminal's protocols makes it useful for testing terminals prior to their commissioning in the INTELSAT TDMA/DSI network.

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John A. Lunsford received a B.S. from the University of Maryland in 1973, and an M.S.E.E. from the University of Pennsylvania in 1980. From 1973 to 1980, he was a Design Engineer in the Advanced Electronic Technology Department at the RCA Missile and Surface Radar Division in Moorestown, N.J. He joined COMSAT Laboratories in 1980, and from 1980 to 1984 was involved in various projects related to the specification and implementation of the INTELSAT 120-Mbit/s TDMA/DSI system. More recently, he was involved in the system design and specification of a 3- to 20-Mbit/s TDMA system for COMSAT Telesystems, Inc. Mr. Lunsford is currently President and Director of Engineering for Neotech, Inc., a young company involved in the implementation of public-access videotext information networks.

Thomas R. Dobyns received a B.S.E.E. from the University of Florida in 1963, and an M.S.E.E. from George Washington University in 1968. He is presently Associate Director of the Network Technology Division at COMSAT Laboratories, where he is responsible for supervising the TDMA network control and TDMA earth terminal design activities for the NASA Advanced Communications Technology Satellite (ACTS) Program. His experience includes TDMA systems and terminal design, on-board baseband processing, and data networking. Mr. Dobyns is a member of IEEE.

Translations of Abstracts

Le système AMRT-CNC INTELSAT

B. A. PONTANO, S. J. CAMPANELLA ET J. L. DICKS

Sommaire

L'article présente une description du système AMRT/concentration numérique des conversations (CNC) à 120 Mbit/s d'INTELSAT. Ce système se compose de terminaux de trafic AMRT, de stations de référence et de surveillance (TRMS) et d'une installation AMRT au Centre d'exploitation INTELSAT (IOCTF). Les performances requises et les caractéristiques des modems associés y sont indiquées. Il contient également une description de l'ensemble du système illustrant le format de paquet et de trame et expliquant les fonctions d'acquisition et de synchronisation. Les auteurs décrivent en outre les caractéristiques techniques et l'interconnexion avec les stations de référence et les terminaux de trafic, ainsi que les jonctions de terminaux de trafic, y compris la CNC. L'IOCTF et ses fonctions de coordination, telles que le changement de plan de trame synchrone, sont expliquées.

Terminal de trafic AMRT expérimental

R. P. RIDINGS, R. R. LINDSTROM ET T. R. DOBYNS

Sommaire

L'article présente les concepts de base, les éléments de conception critiques et les critères de mise en oeuvre d'un terminal de trafic expérimental d'accès multiple par répartition dans le temps (AMRT) à 120 Mbit/s mis au point par les Laboratoires COMSAT suivant les spécifications d'INTELSAT contenues dans le document BG-42-65 (Rév. 2). Le terminal se compose d'un dispositif de gestion AMRT, d'un modem, d'un module de concentration numérique des conversations (CNC) et d'appareils d'essai speciaux. L'architecture du dispositif de gestion AMRT, le pupitre de l'opérateur, l'interface CNC, et d'appareils d'essai spéciaux y sont illustrés. Les appareils d'essai spéciaux se composent d'un générateur de paquets de référence et d'un dispositif de mesure du taux d'erreur sur les bits et de l'intervalle sans erreur (TEB/SE). Le générateur de paquets de référence permet les essais en configuration en boucle par satellite. Compte tenu surtout du détecteur de mot unique (MU) et du